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(12) **United States Patent**
Pellizzer

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(45) **Date of Patent: May 17, 2016**

(54) **MEMORY ARRAYS WITH POLYGONAL MEMORY CELLS HAVING SPECIFIC SIDEWALL ORIENTATIONS**

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(51) **Int. Cl.**
H01L 27/24 (2006.01)
H01L 45/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/2463*** (2013.01); ***H01L 45/06*** (2013.01); ***H01L 45/1233*** (2013.01); ***H01L 45/144*** (2013.01); ***H01L 45/1666*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 27/249; H01L 45/1675; H01L 45/1253; H01L 45/085; H01L 45/143; H01L 27/2436; H01L 45/08; H01L 45/144; H01L 45/147; H01L 45/14; H01L 45/04; H01L 45/146; H01L 45/1226; H01L 45/142; G11C 13/0002; G11C 13/0011
USPC 257/208, E23.141, E21.645; 438/128
See application file for complete search history.

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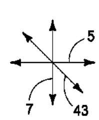
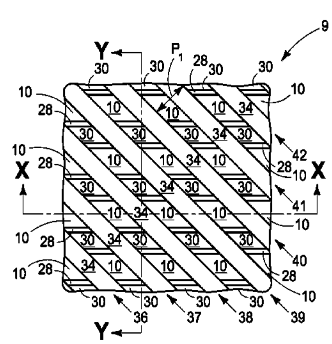
(74) *Attorney, Agent, or Firm* — Wells St. John P.S.

(57) **ABSTRACT**

Some embodiments include a memory array having a first series of access/sense lines which extend along a first direction, a second series of access/sense lines over the first series of access/sense lines and which extend along a second direction substantially orthogonal to the first direction, and memory cells vertically between the first and second series of access/sense lines. Each memory cell is uniquely addressed by a combination of an access/sense line from the first series and an access/sense line from the second series. The memory cells have programmable material. At least some of the programmable material within each memory cell is a polygonal structure having a sidewall that extends along a third direction which is different from the first and second directions. Some embodiments include methods of forming memory arrays.

15 Claims, 48 Drawing Sheets





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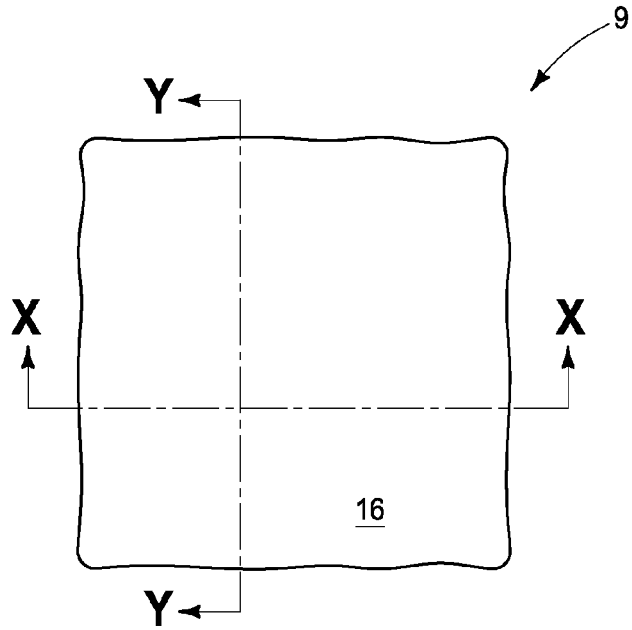

FIG. 1

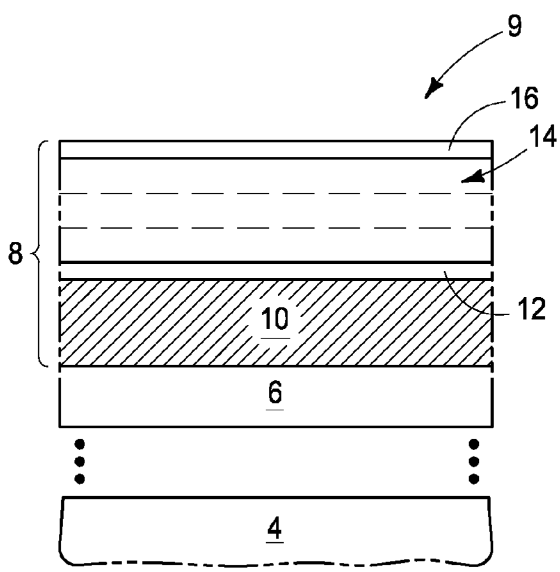

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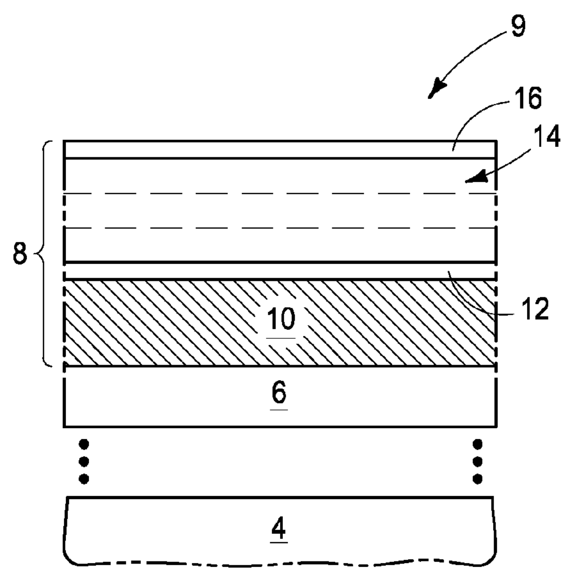
FIG. 1A



Y-Y
FIG. 1B

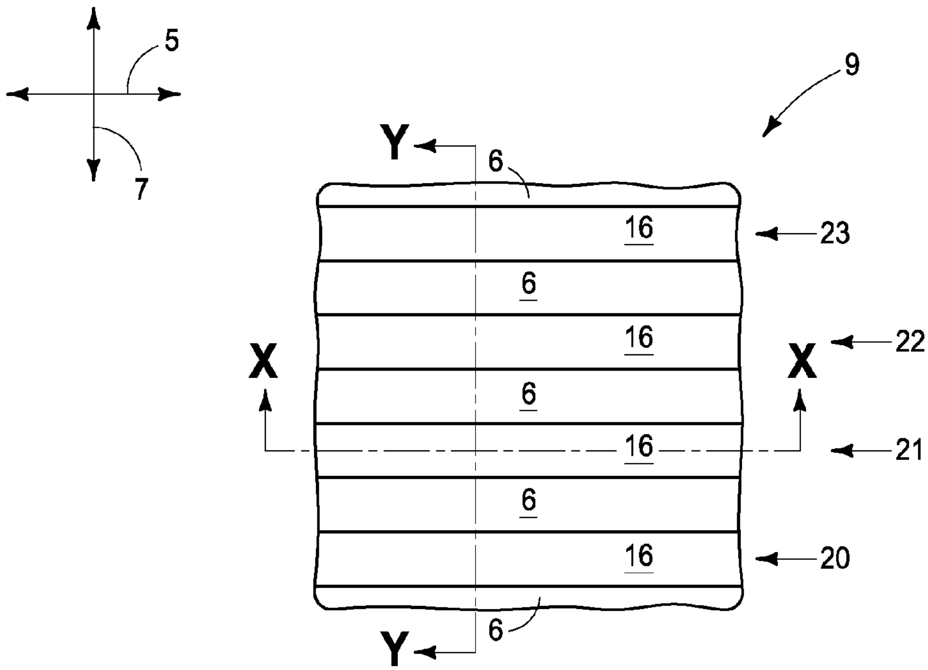


FIG. 2

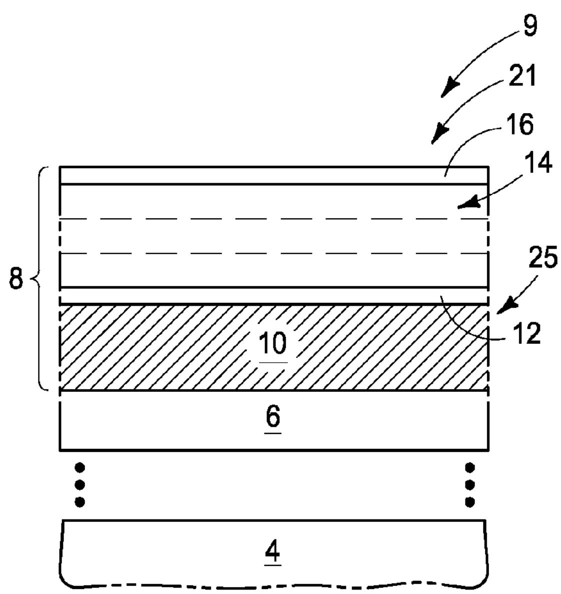


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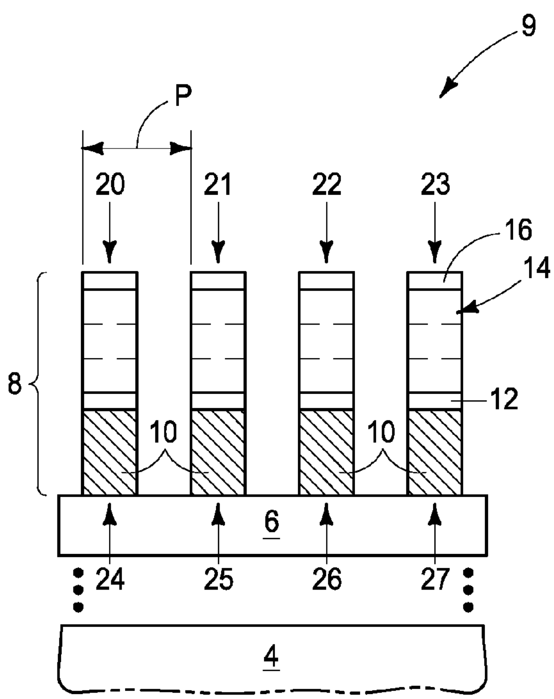
FIG. 2A



Y-Y
FIG. 2B

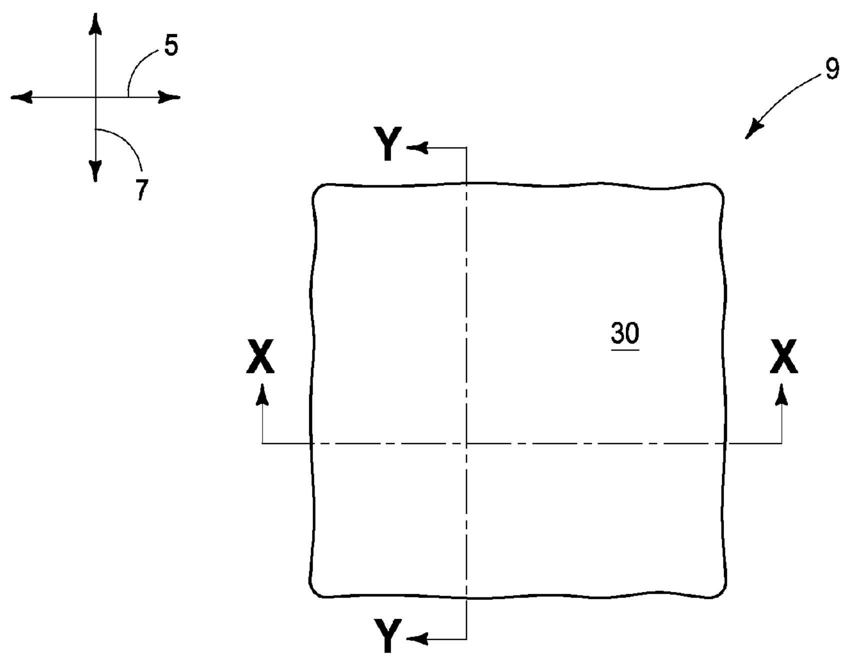


FIG. 3

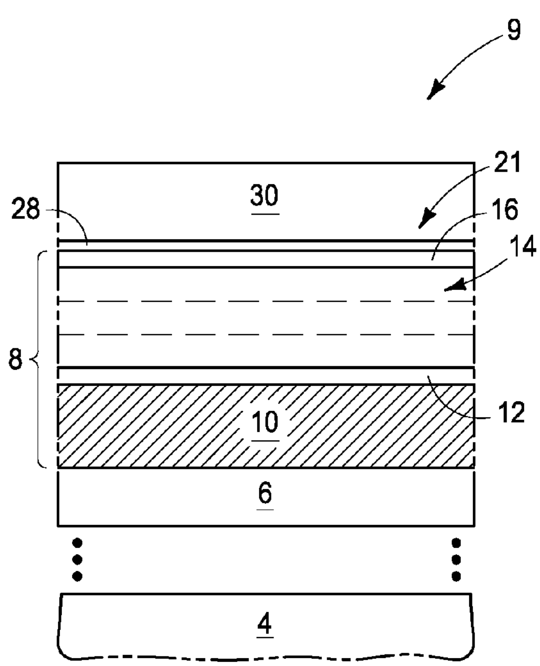


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FIG. 3A

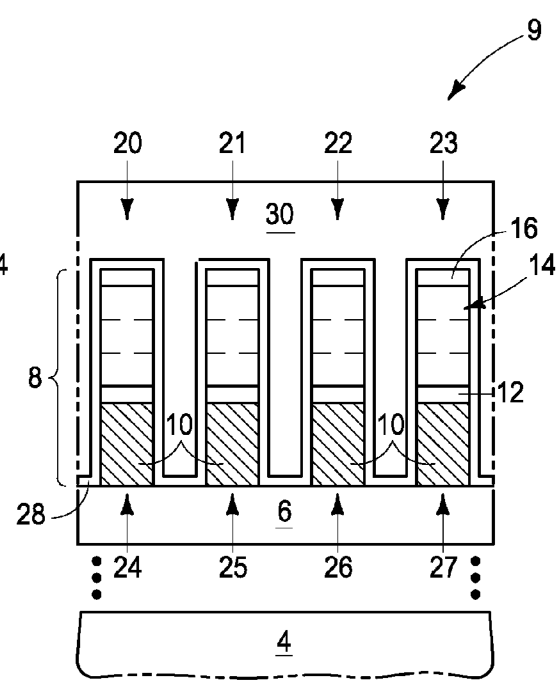

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FIG. 3B

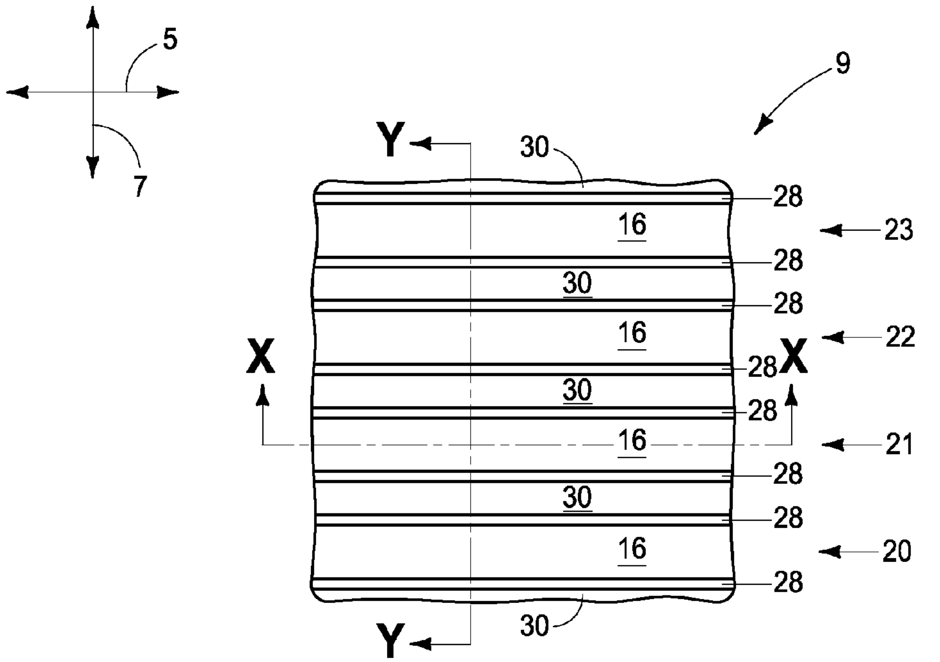

FIG. 4

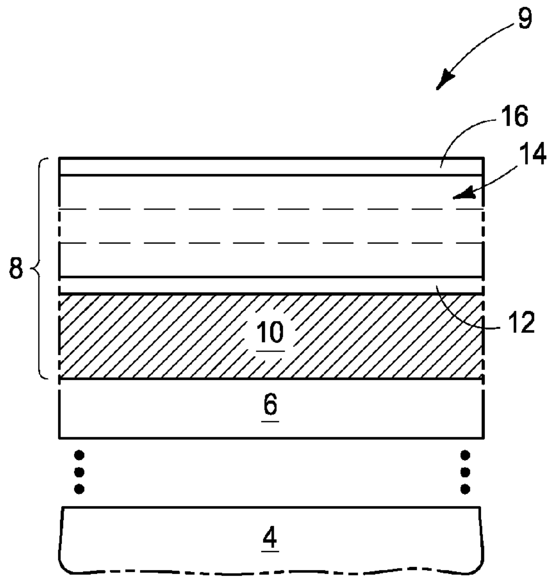

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FIG. 4A

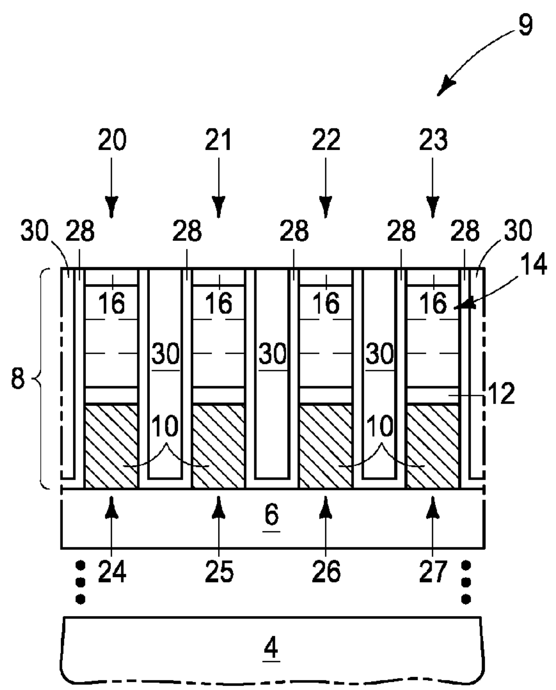

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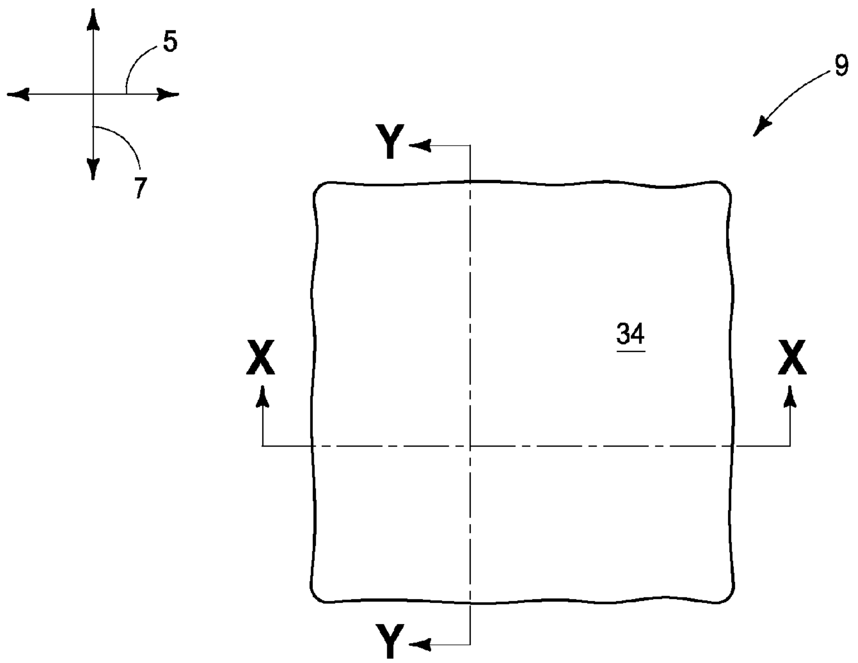
FIG. 4B



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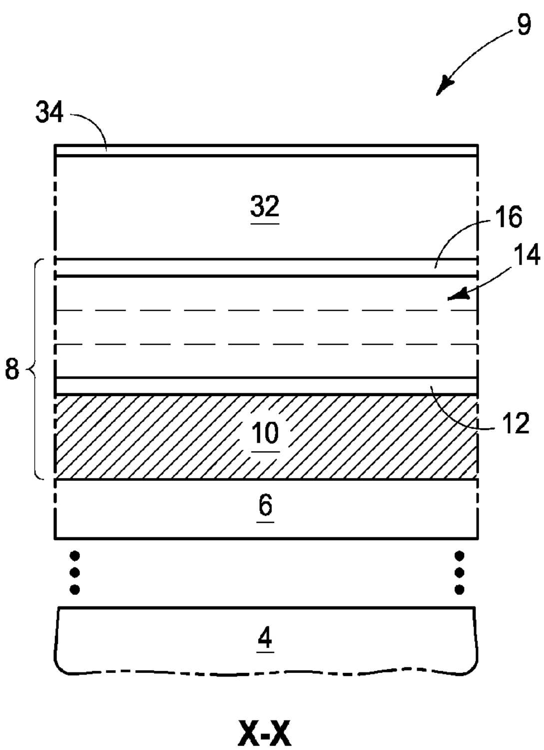


FIG. 5A

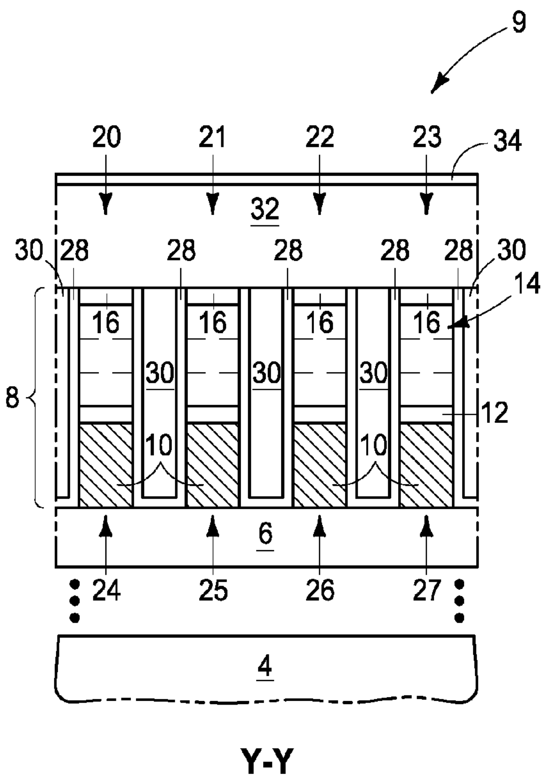
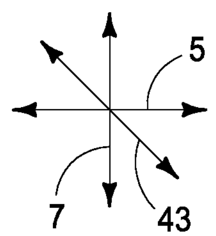


FIG. 5B



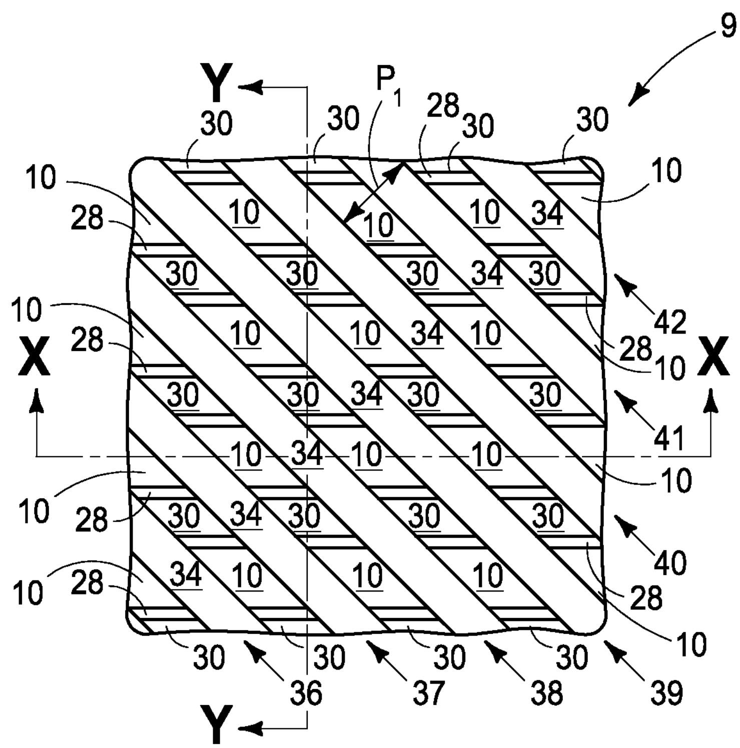


FIG. 6

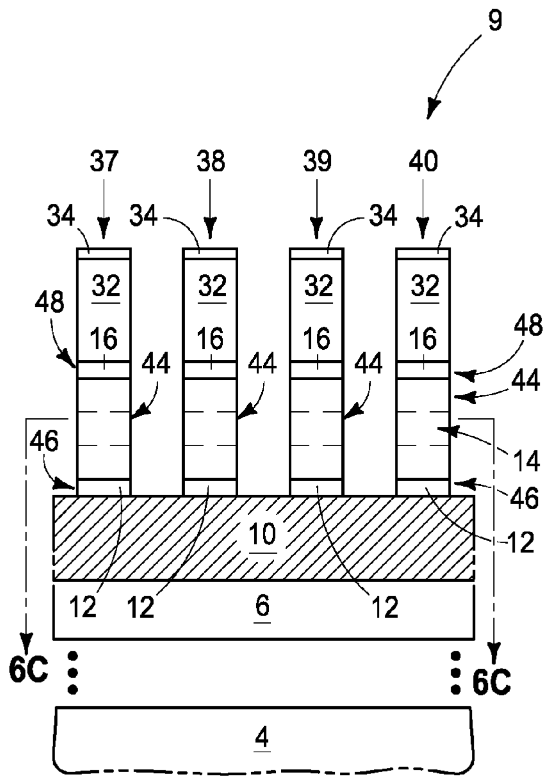


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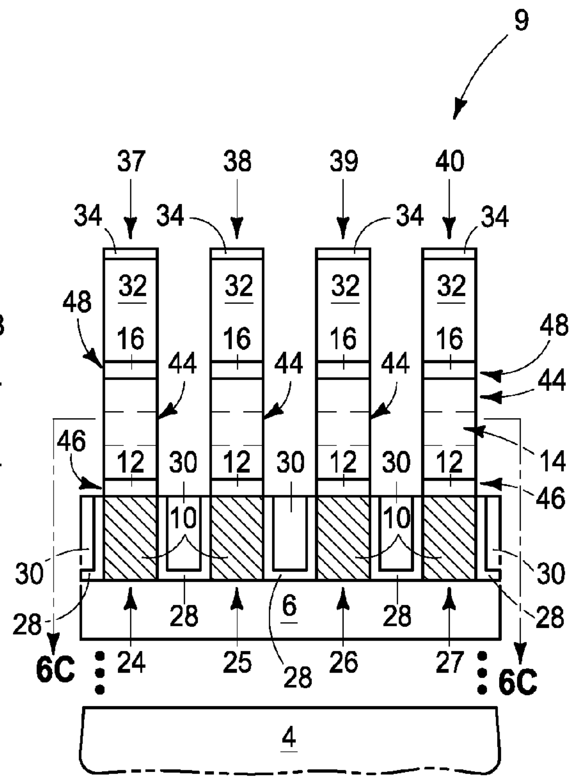
FIG. 6A



Y-Y
FIG. 6B

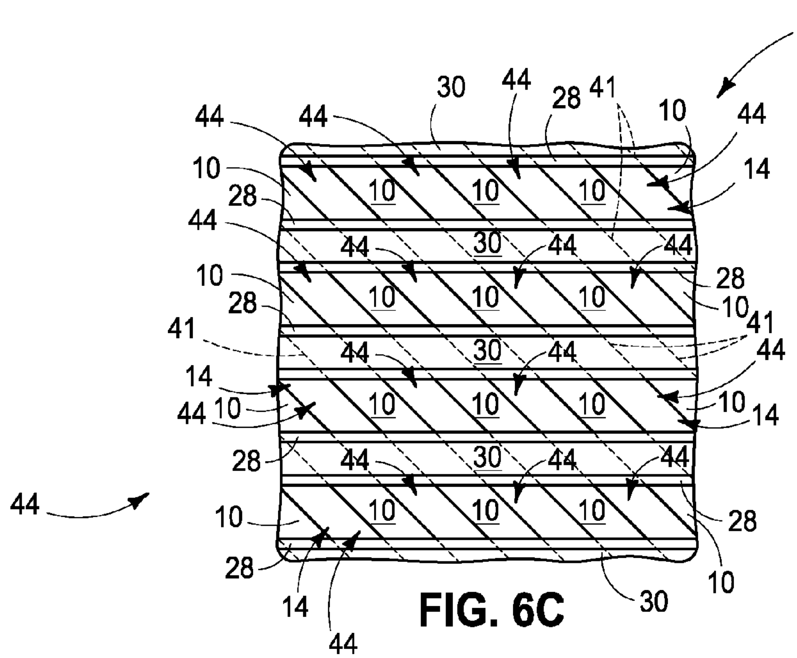
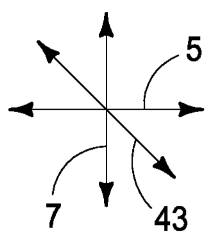


FIG. 6C



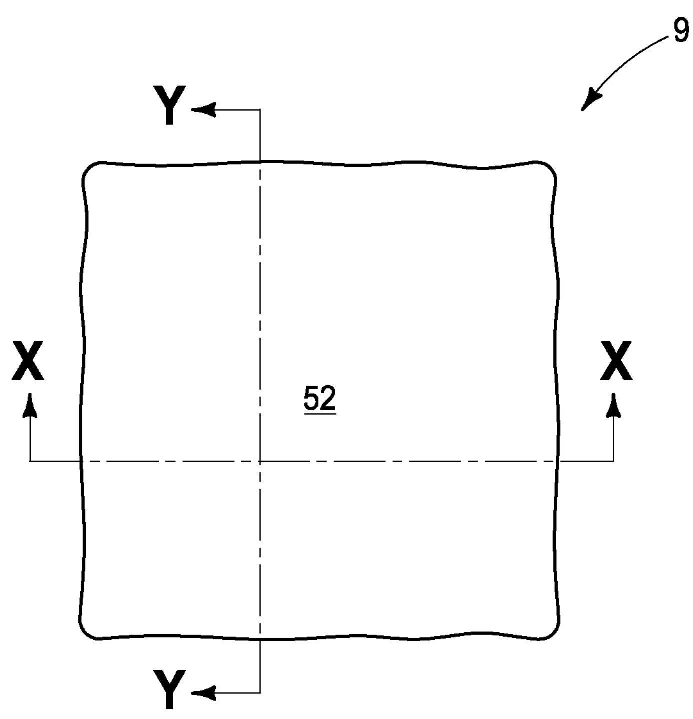


FIG. 7

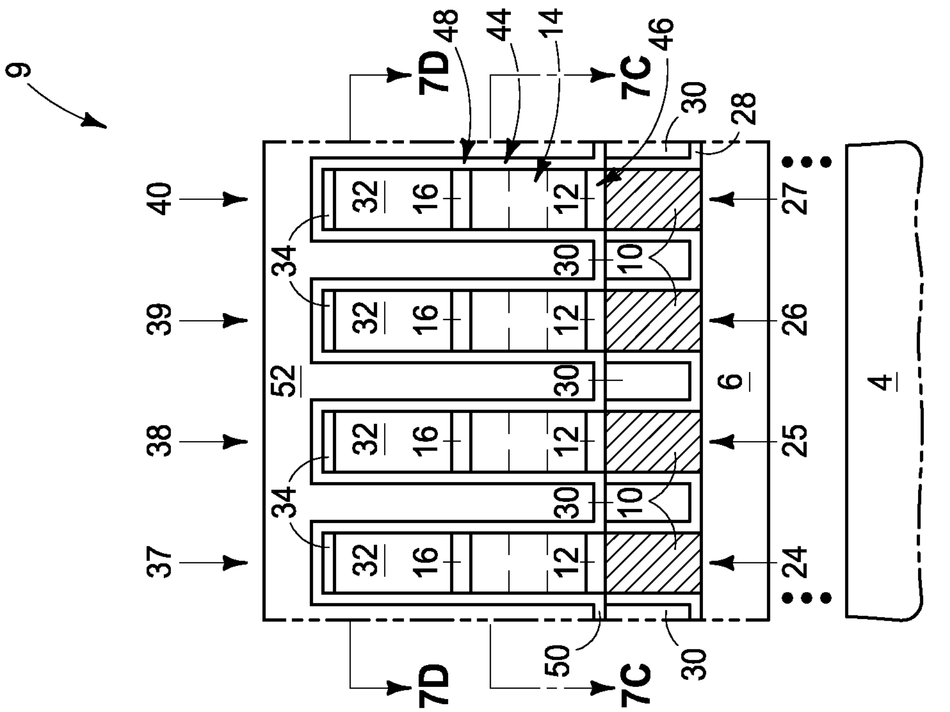


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FIG. 7B

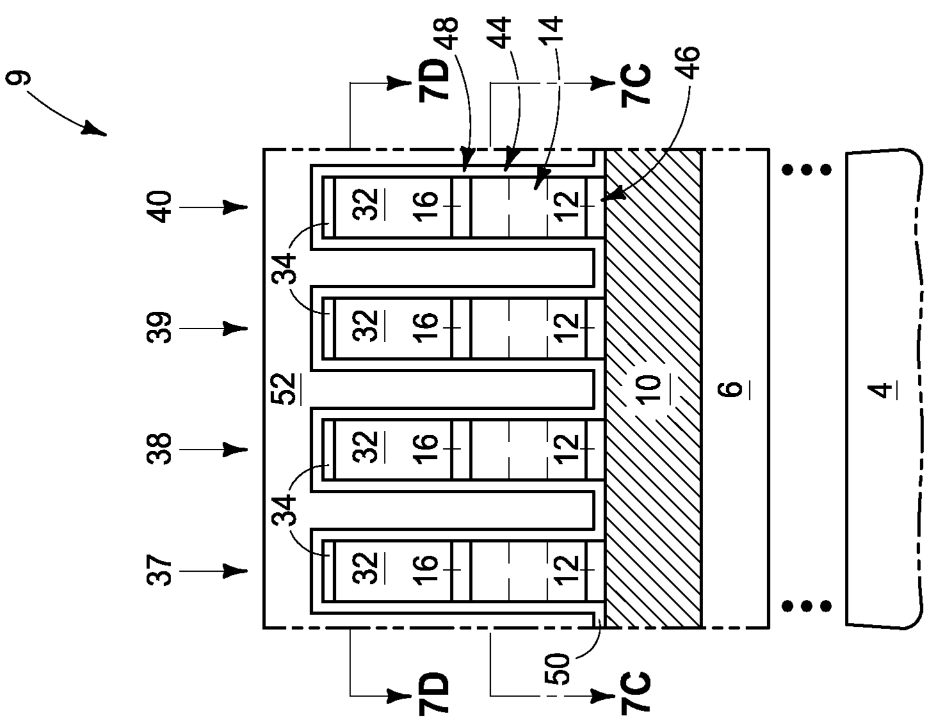

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FIG. 7A

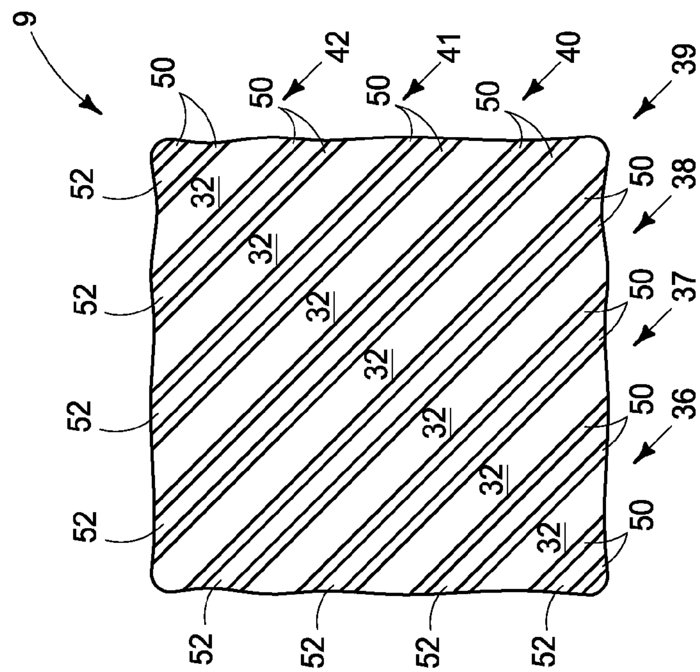


FIG. 7D

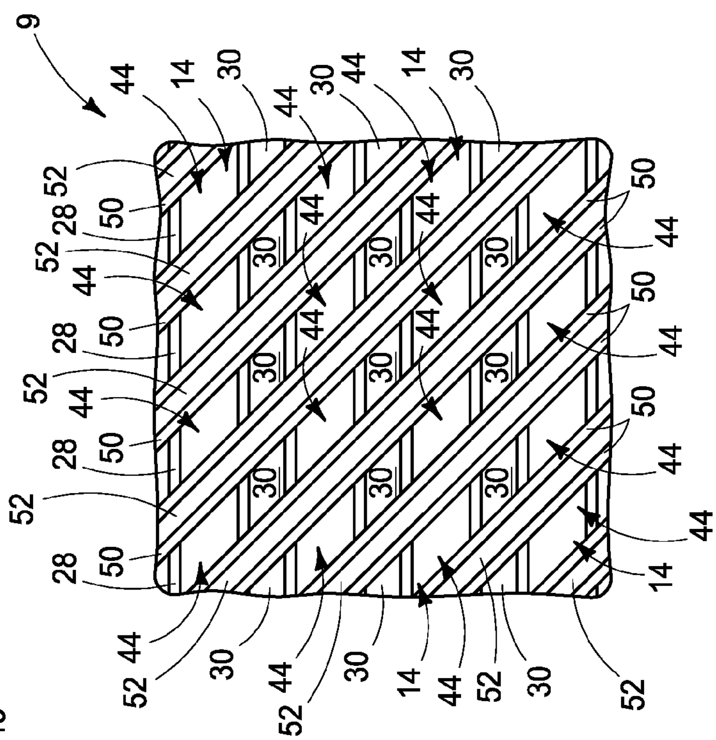
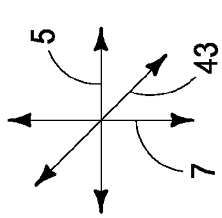
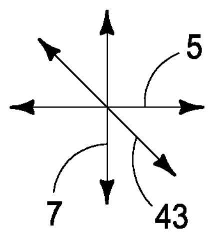


FIG. 7C

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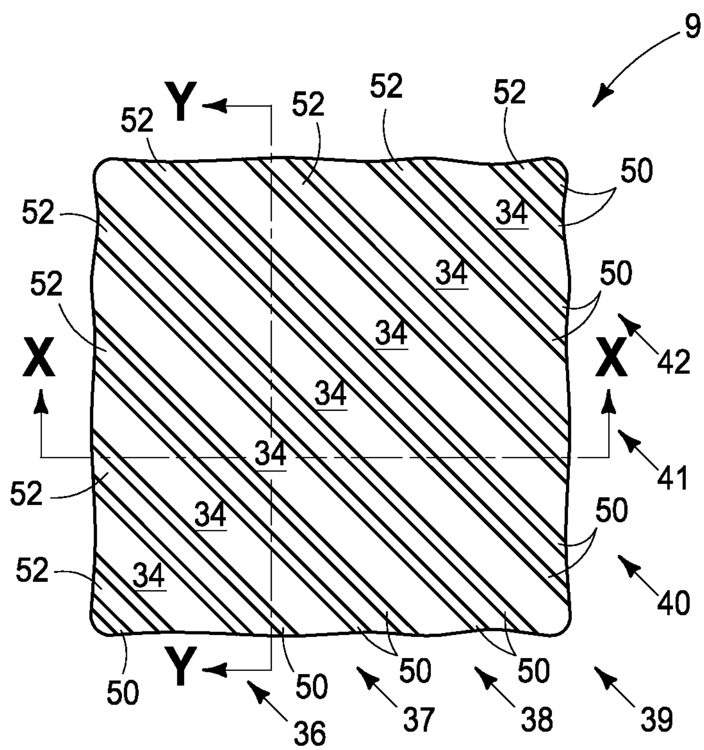
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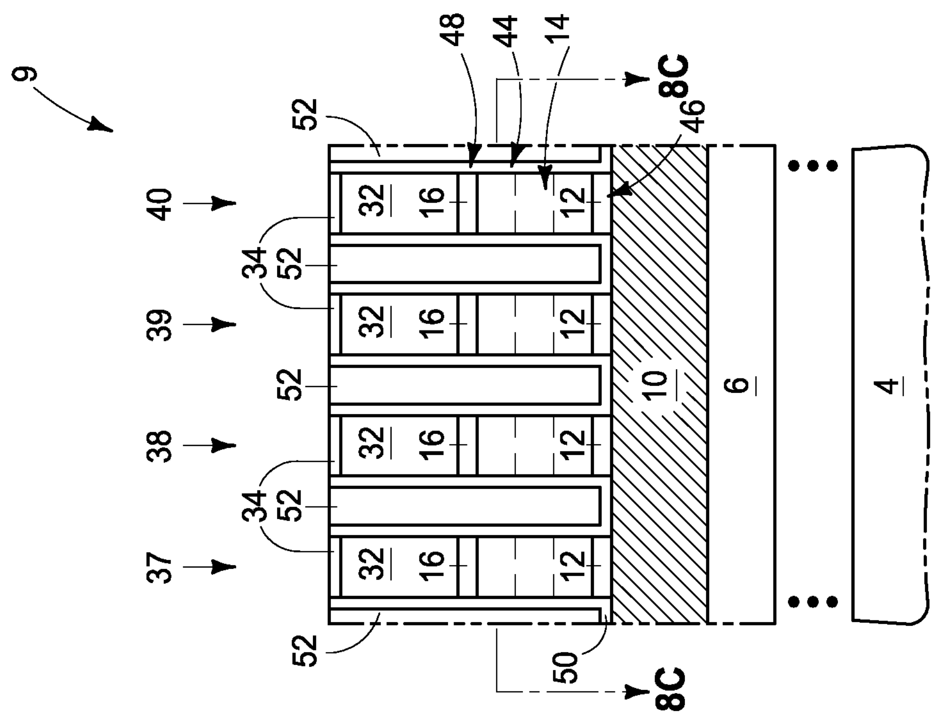
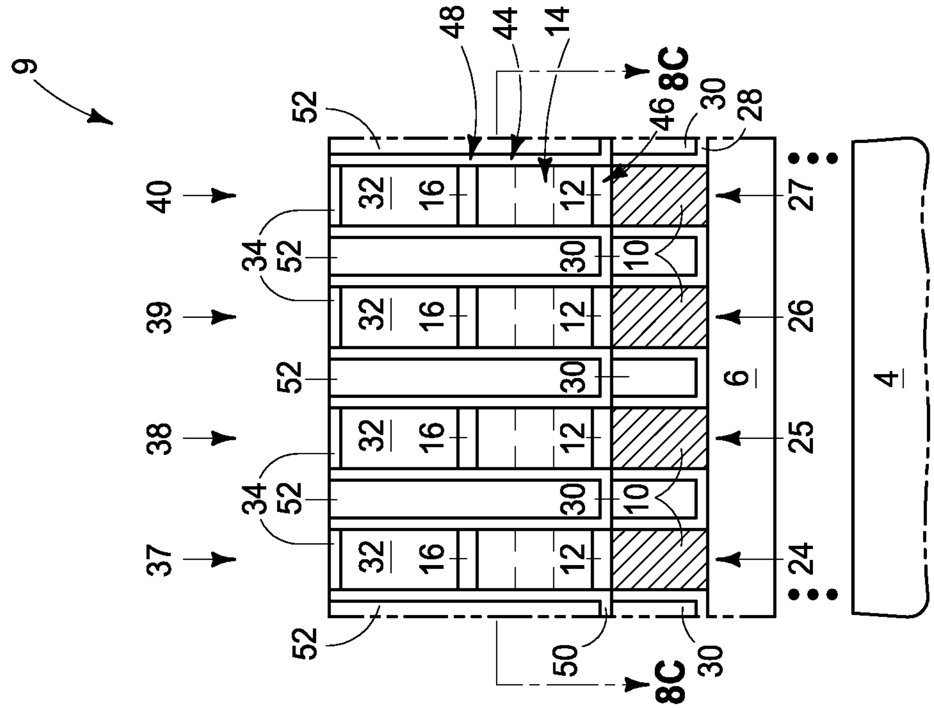
FIG. 8



X-X
FIG. 8A



Y-Y
FIG. 8B

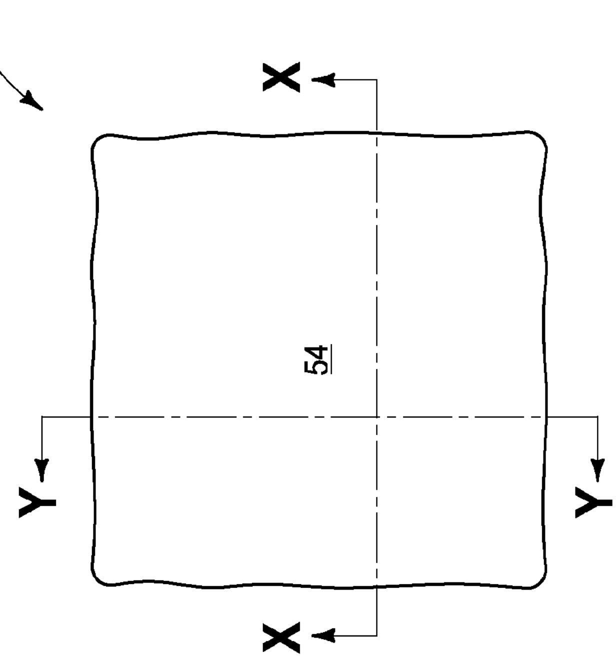


FIG. 9

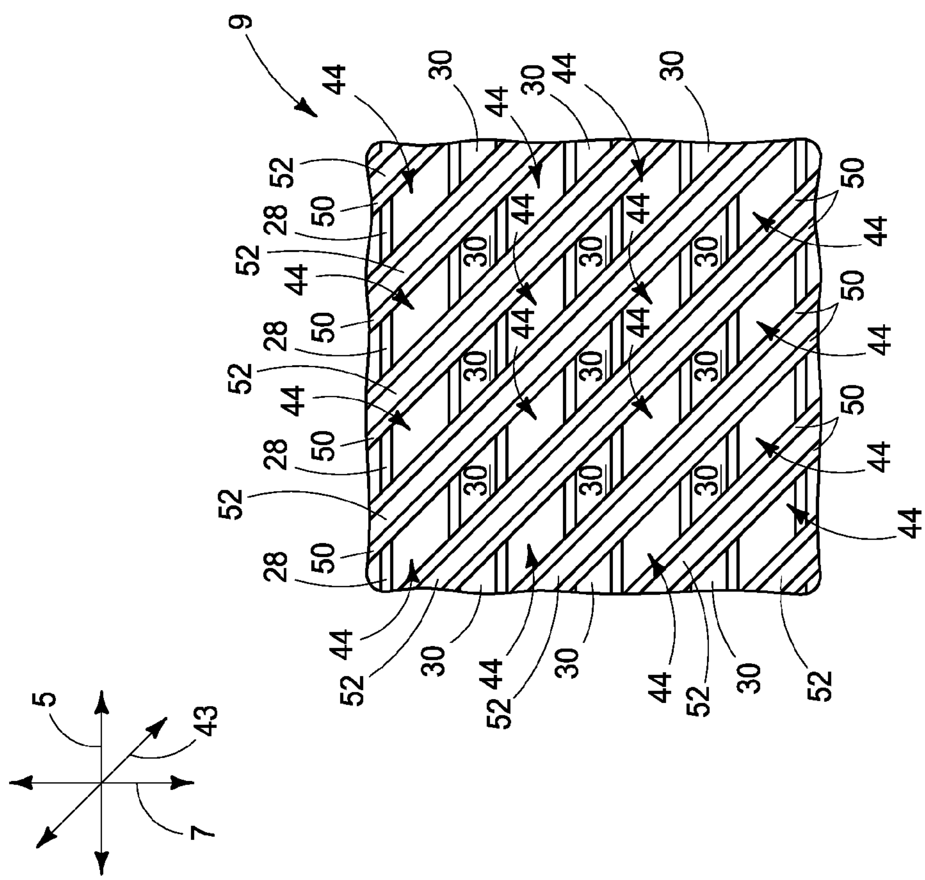
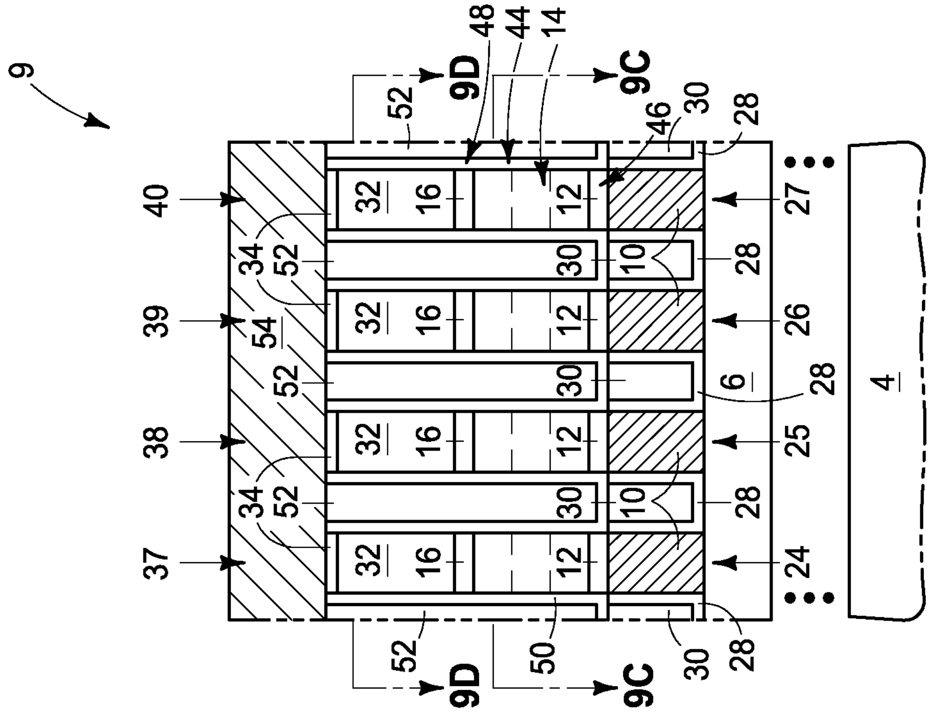
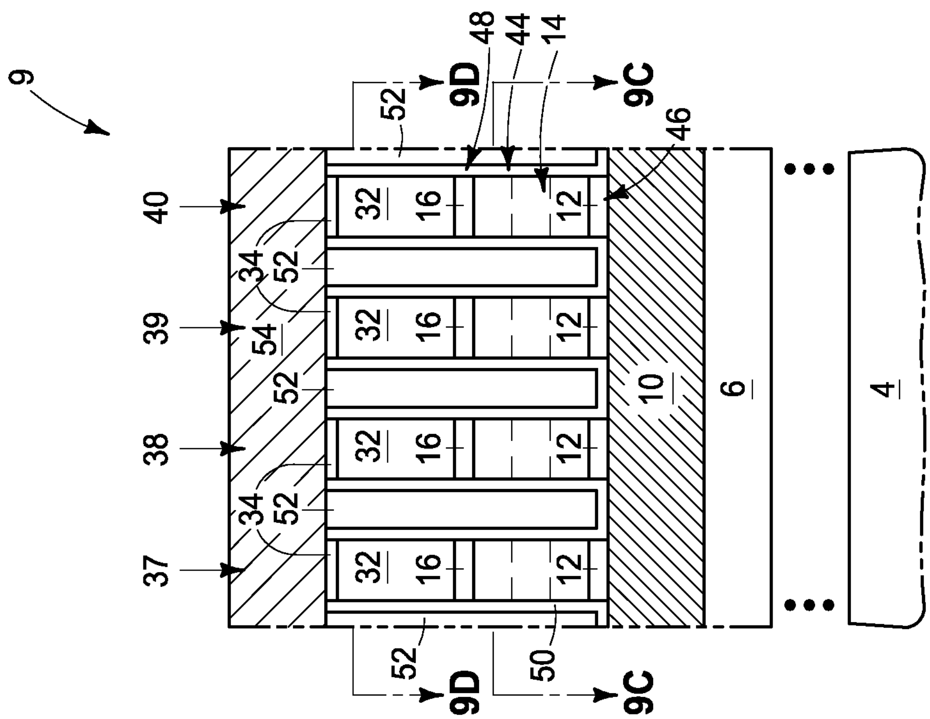


FIG. 8C



Y-Y
FIG. 9B



X-X
FIG. 9A

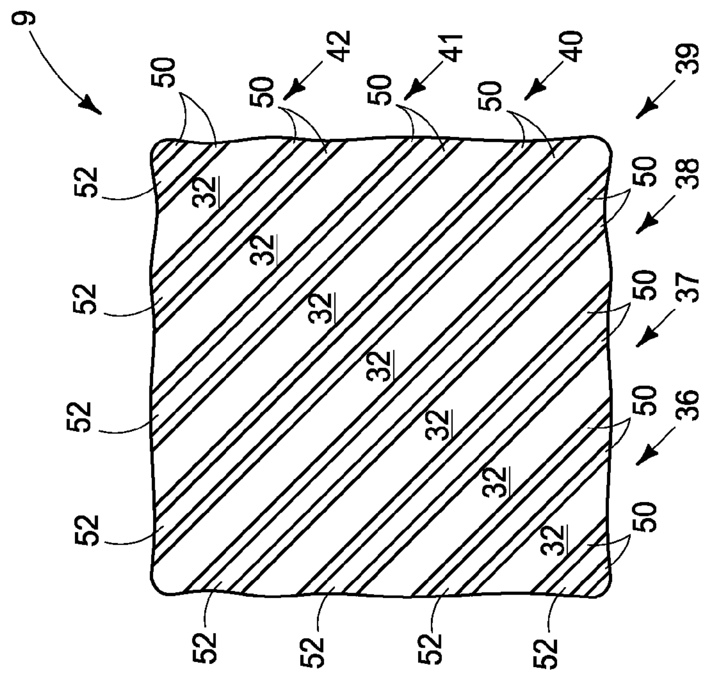


FIG. 9D

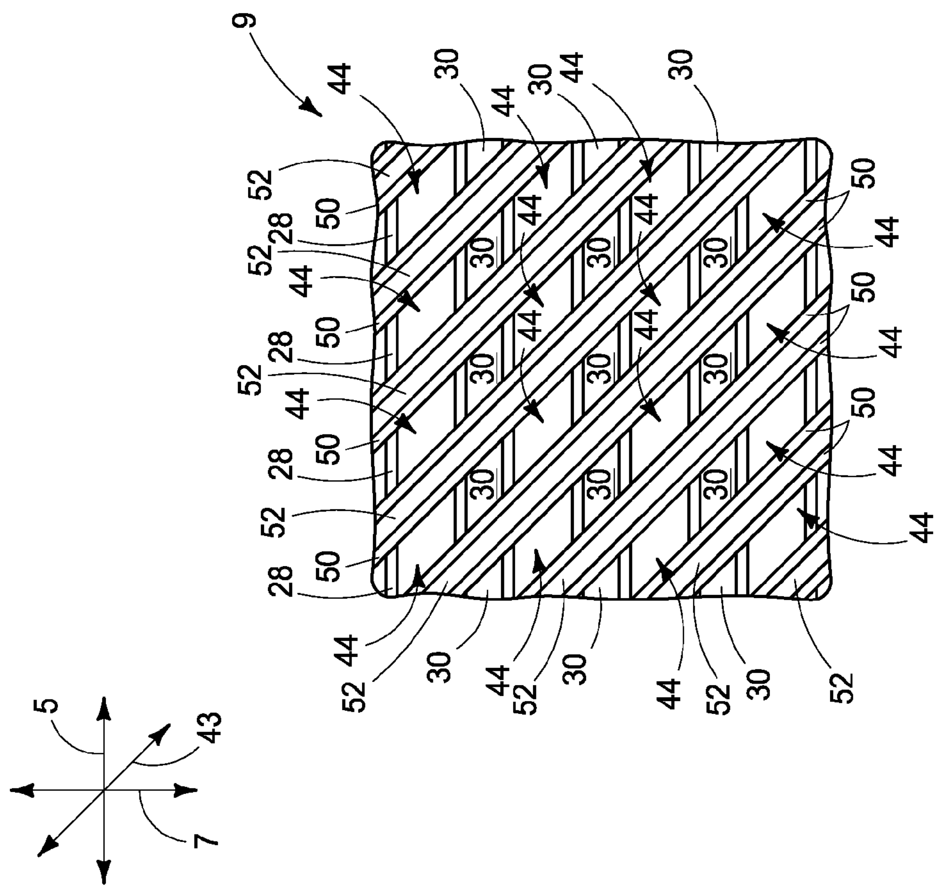
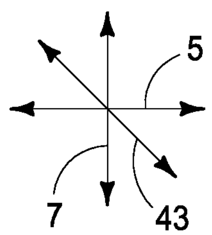


FIG. 9C



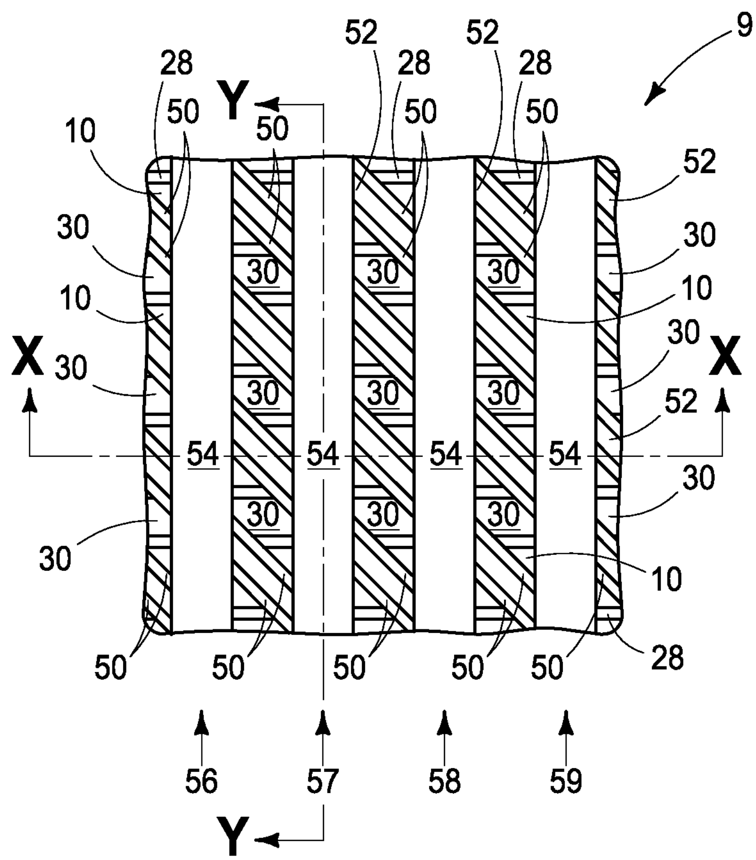
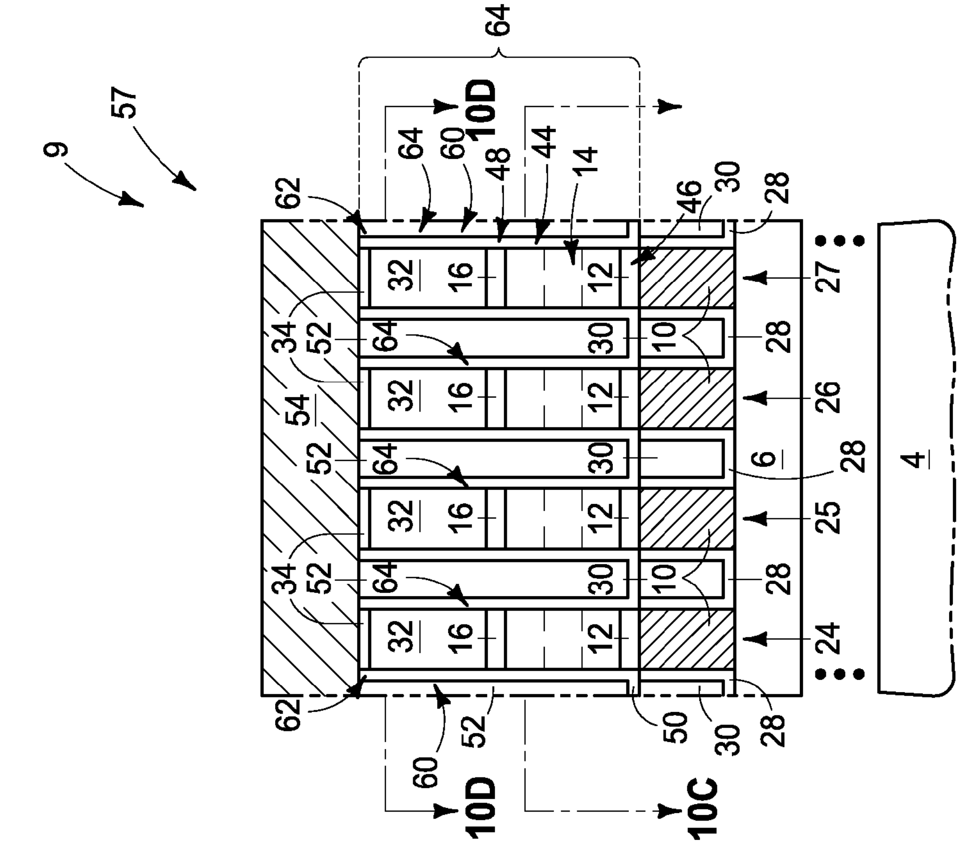
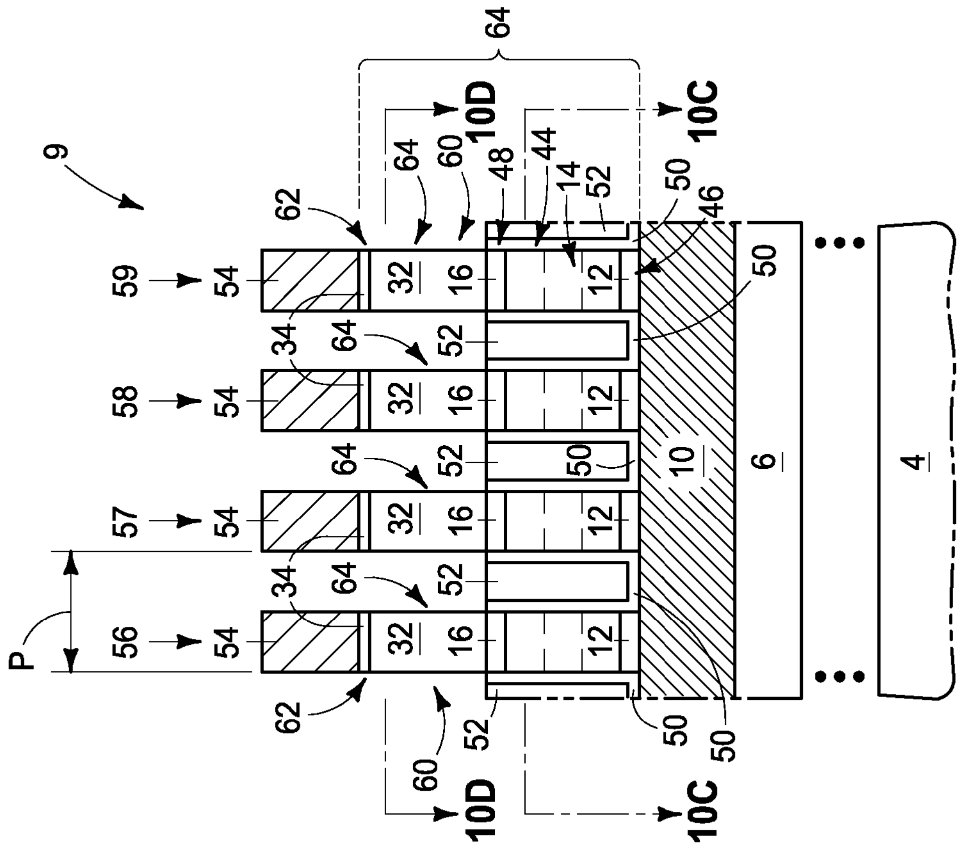


FIG. 10



Y-Y
FIG. 10B



X-X
FIG. 10A

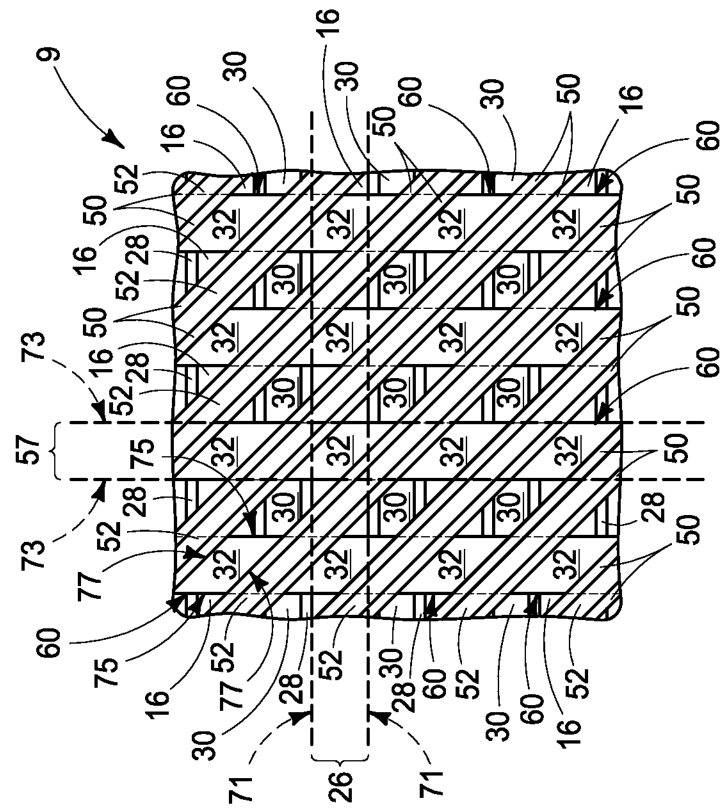


FIG. 10D

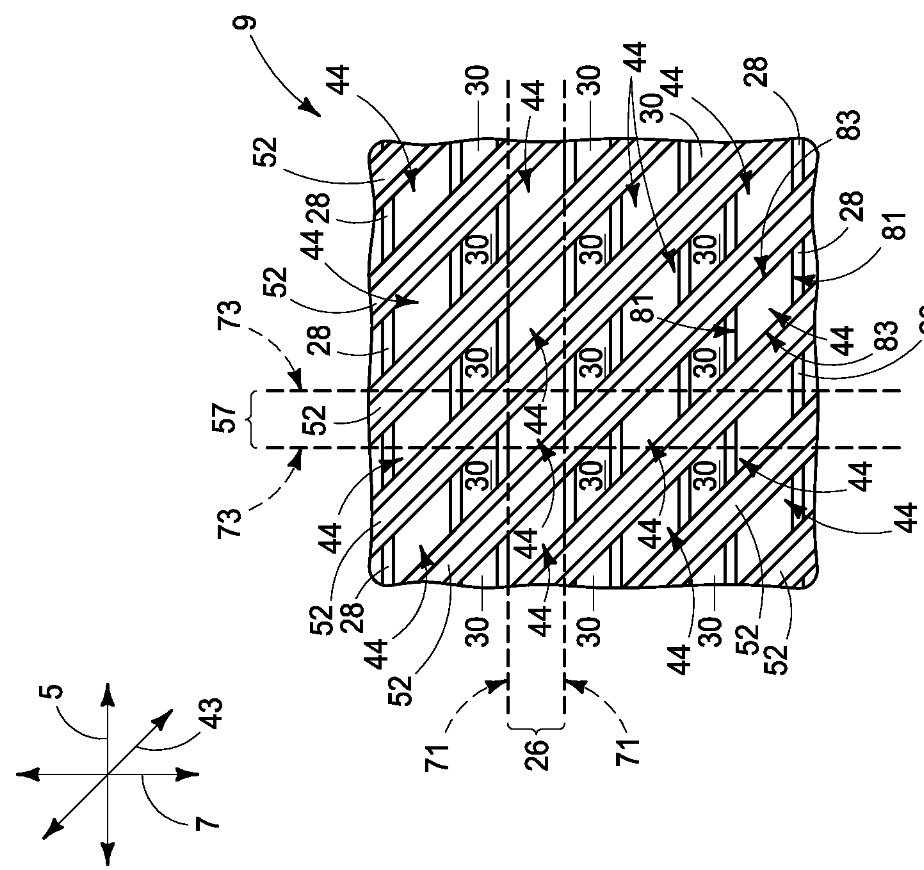
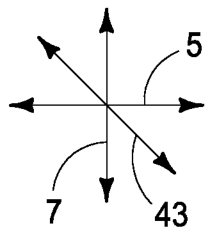


FIG. 10C



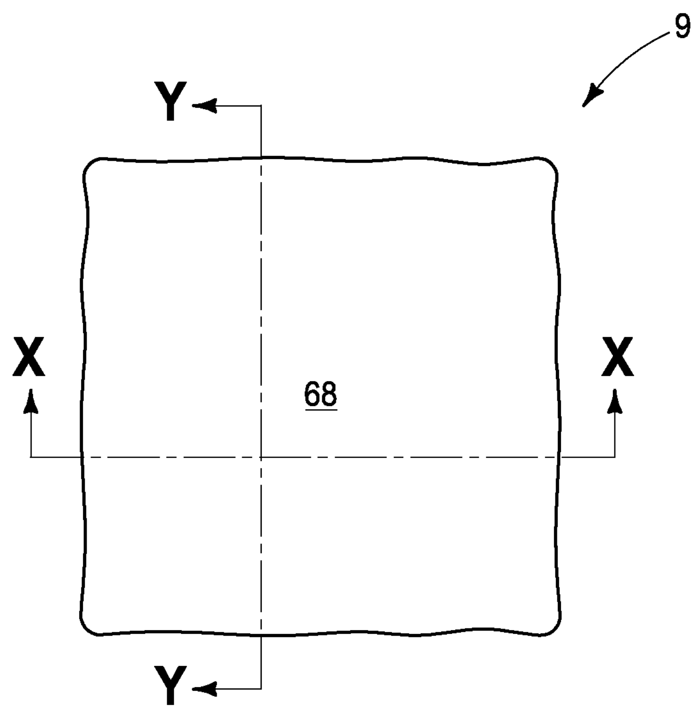
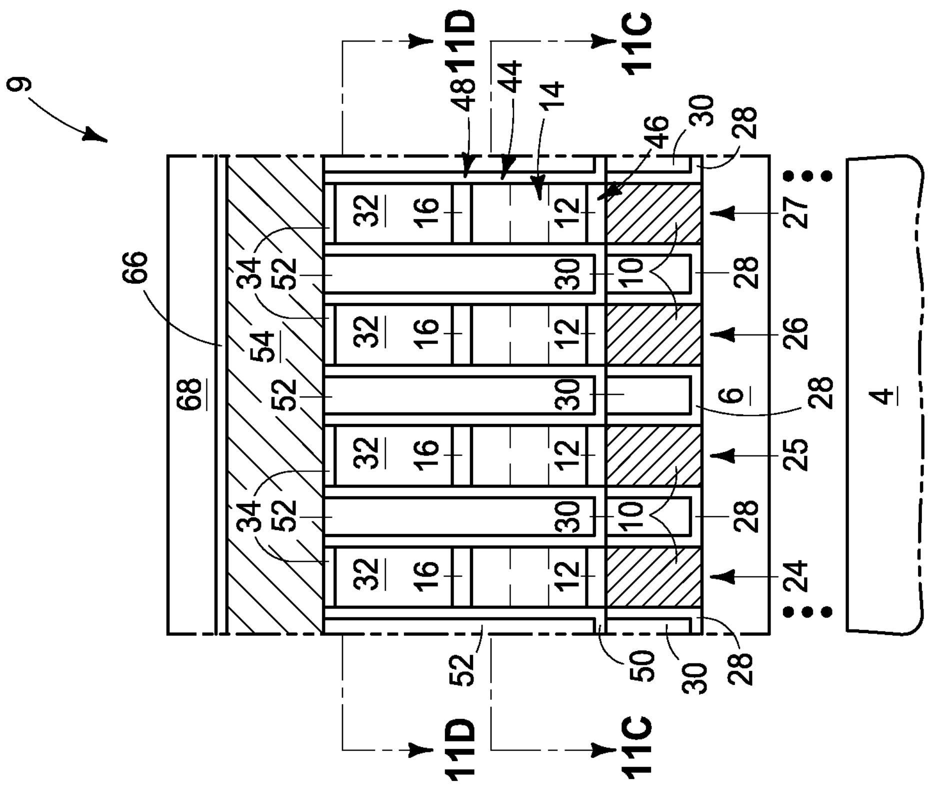
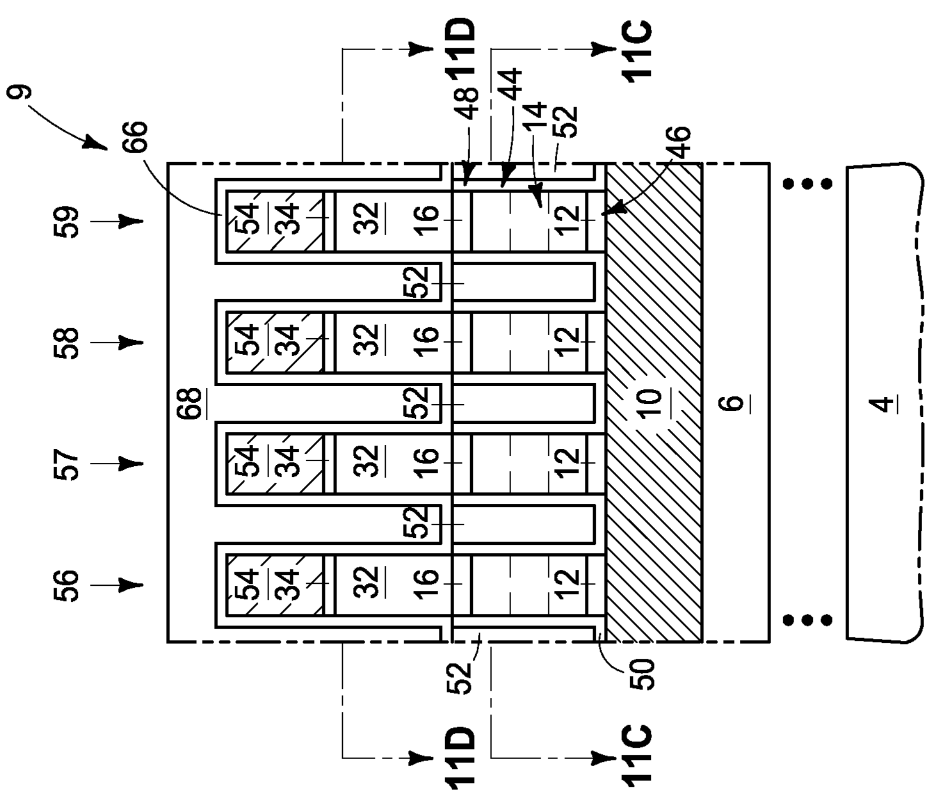


FIG. 11



Y-Y
FIG. 11B



X-X
FIG. 11A

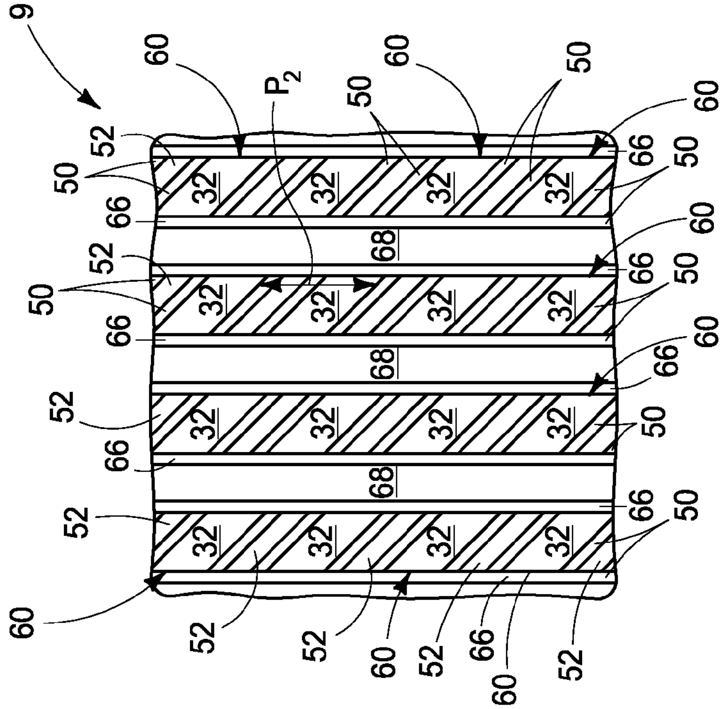


FIG. 11D

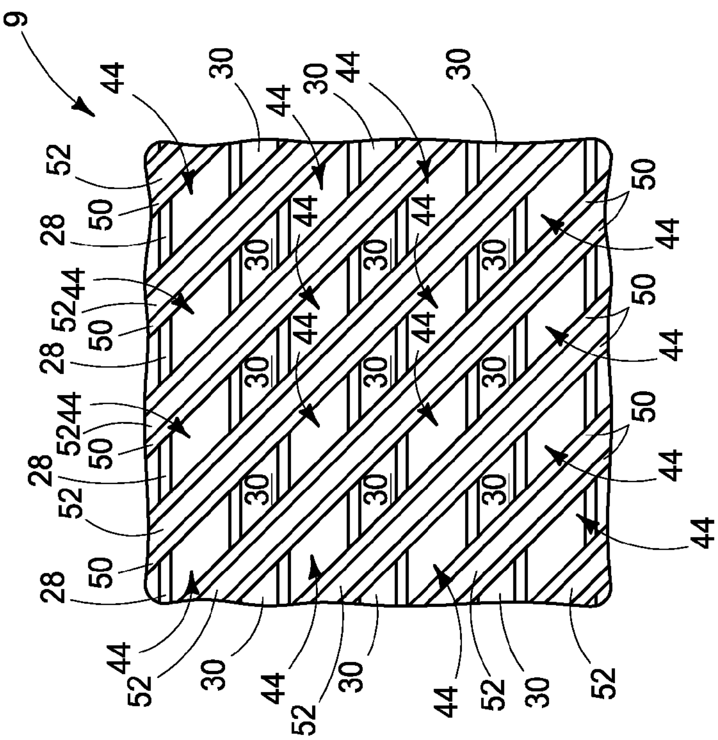
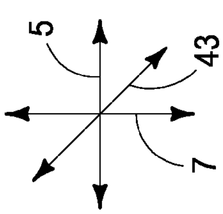
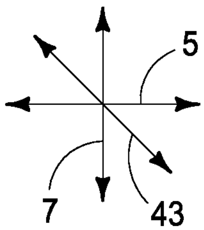


FIG. 11C





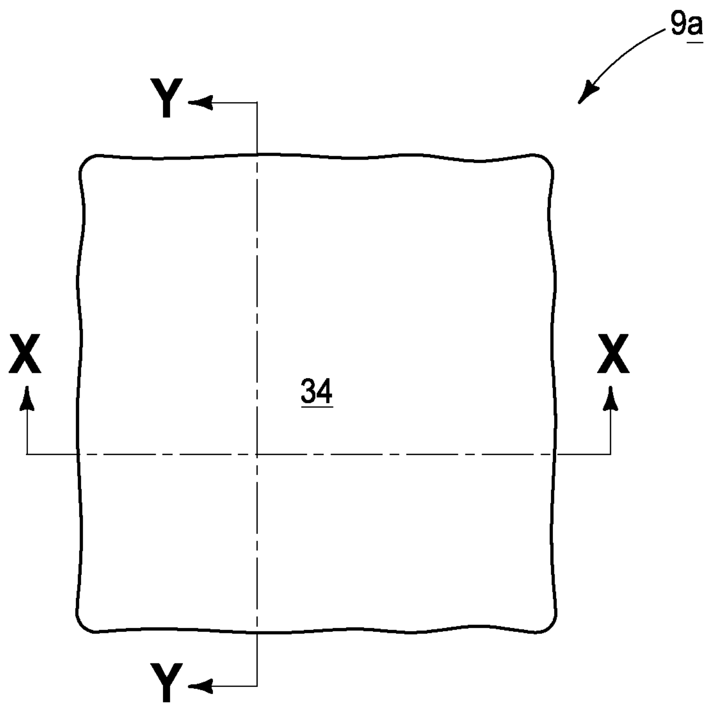
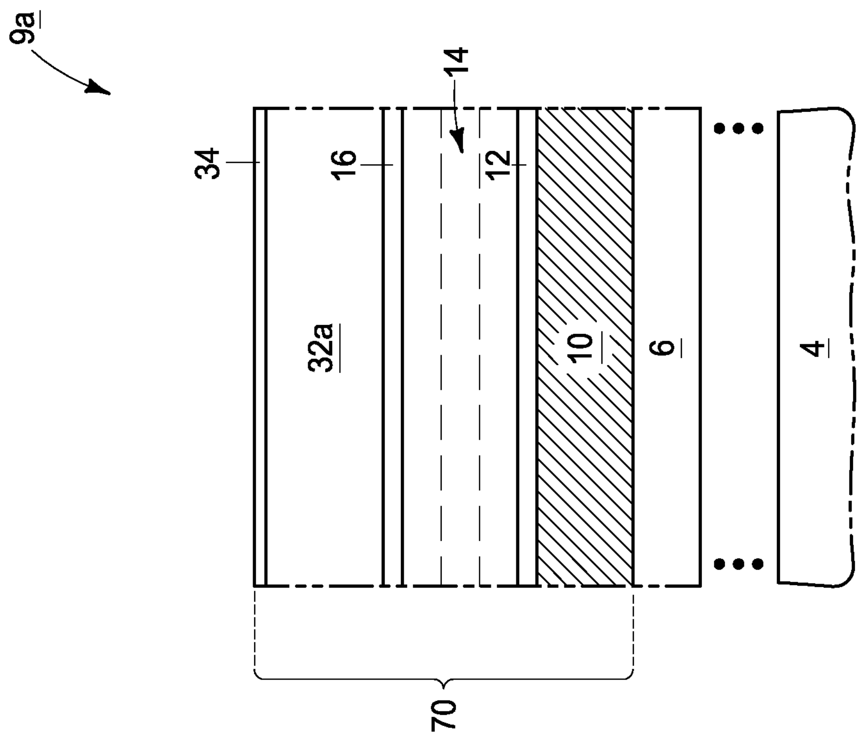
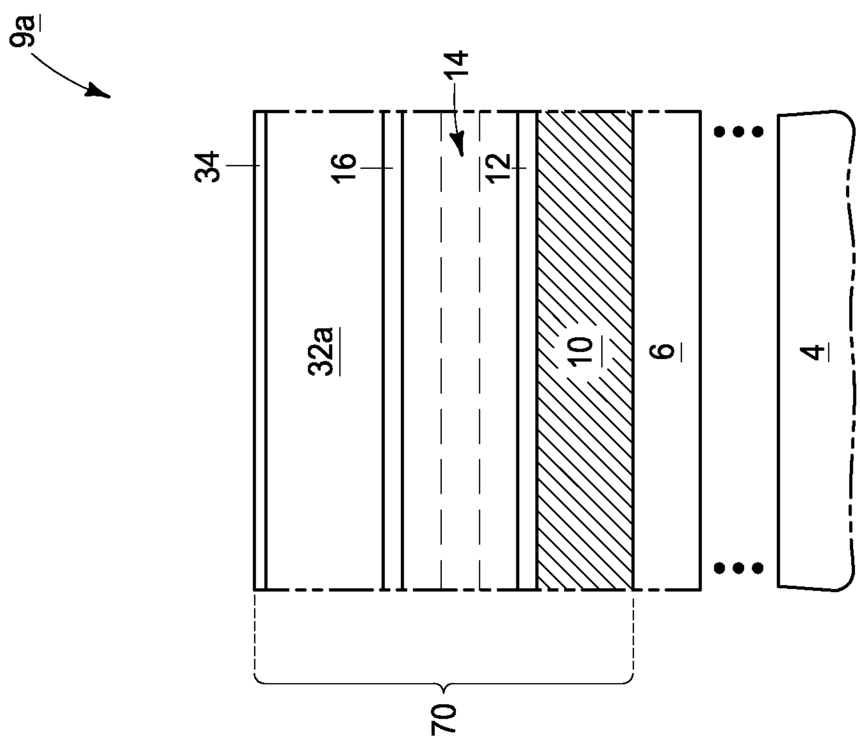


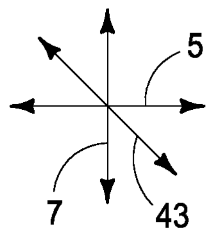
FIG. 12



Y-Y
FIG. 12B



X-X
FIG. 12A



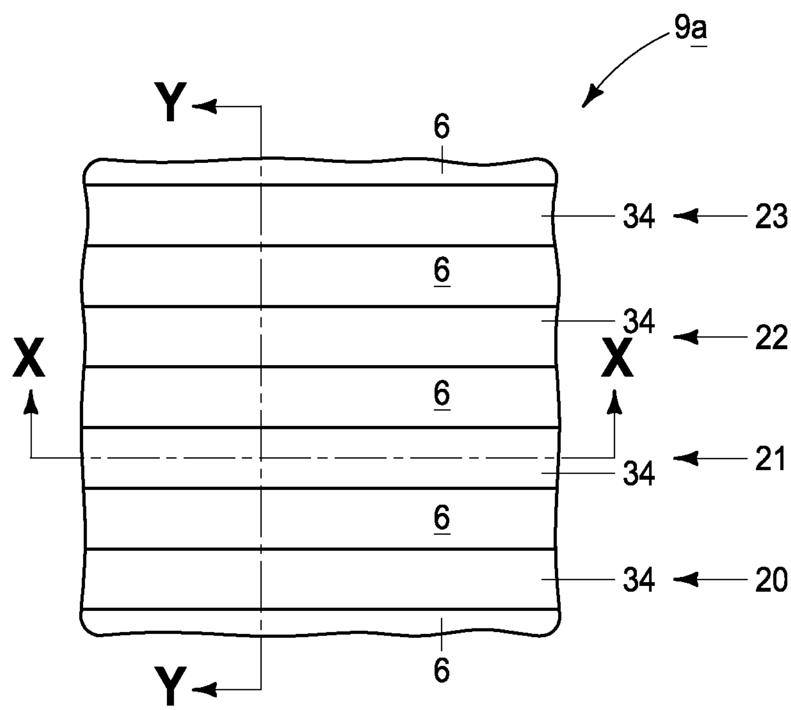
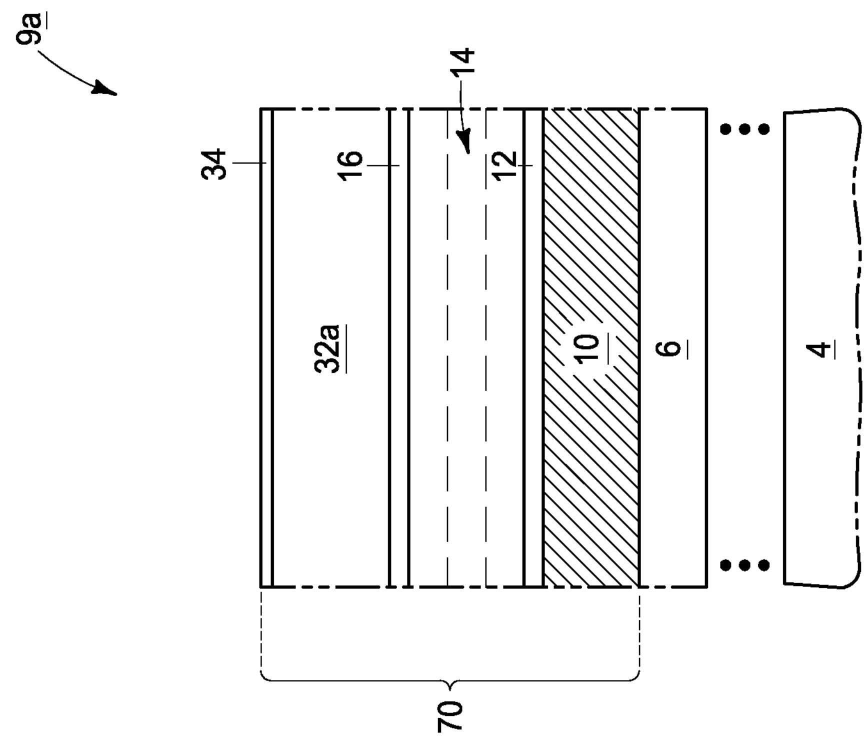
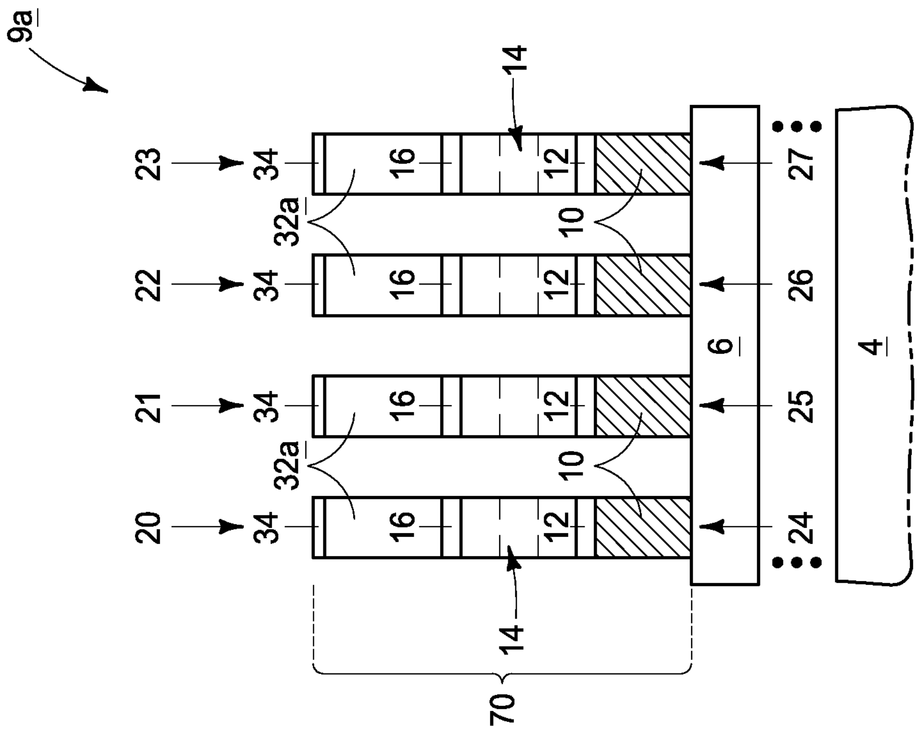


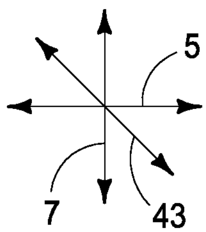
FIG. 13



X-X
FIG. 13A



Y-Y
FIG. 13B



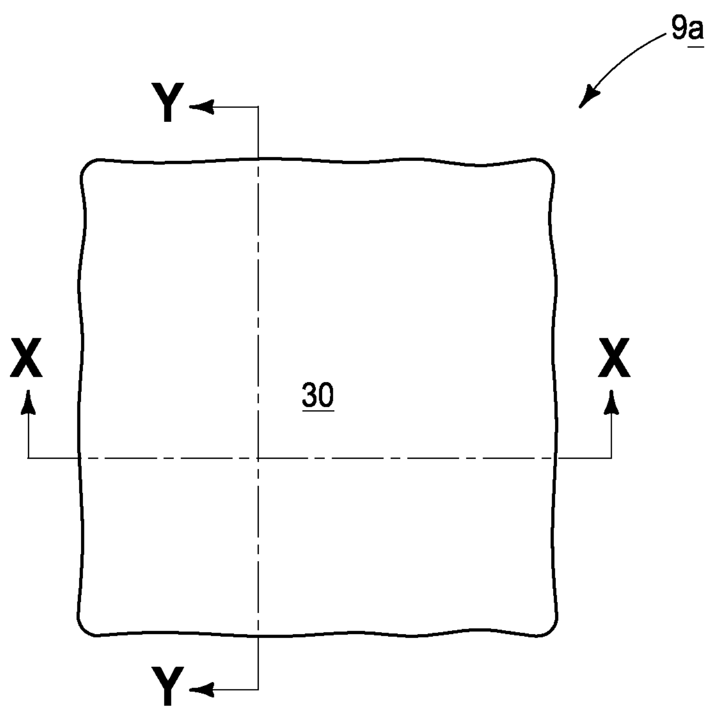
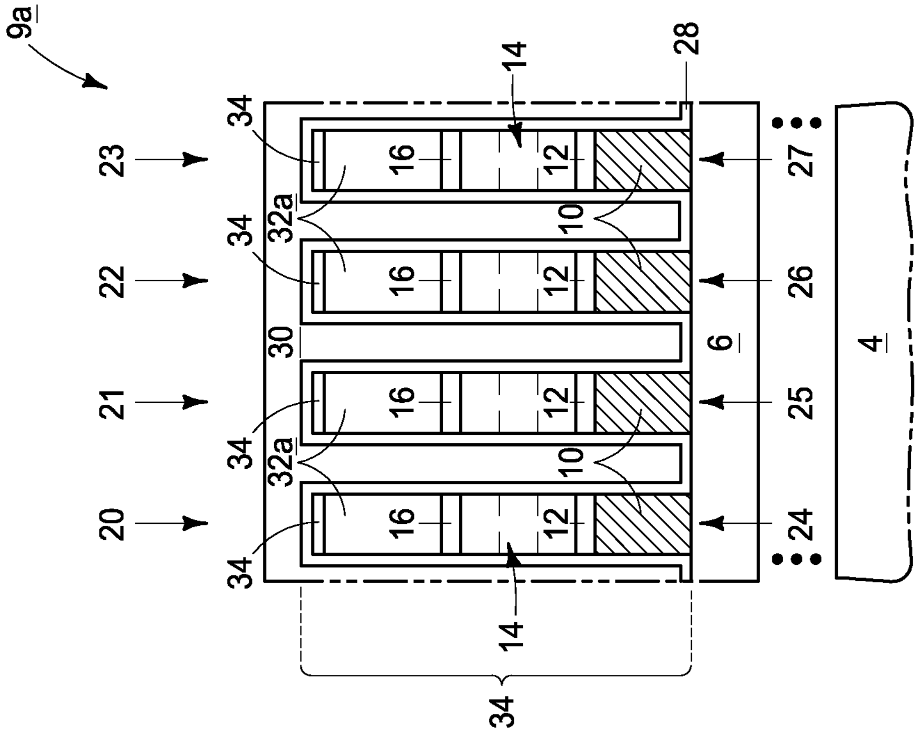
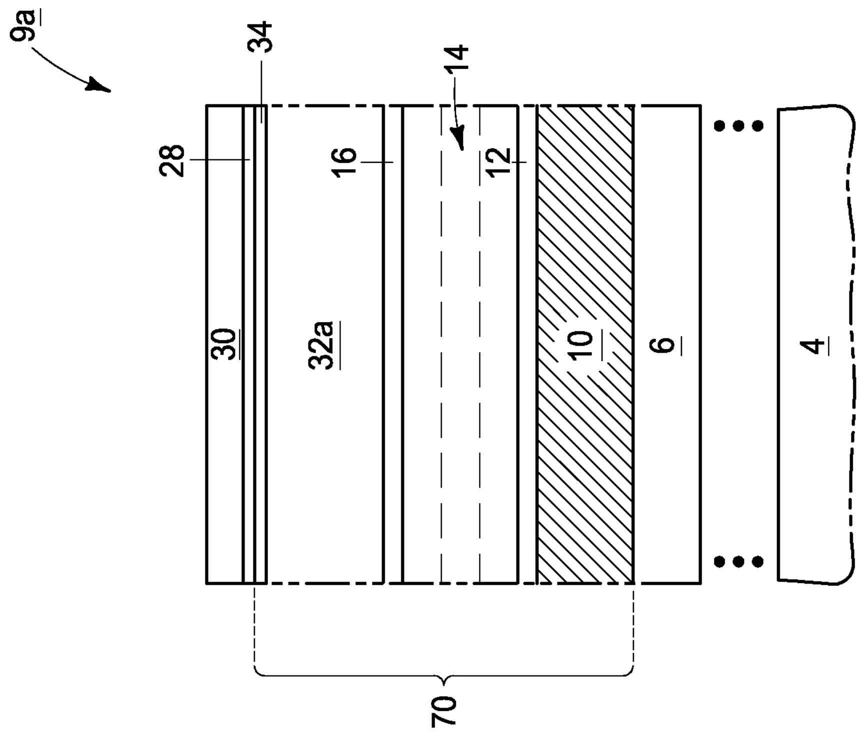


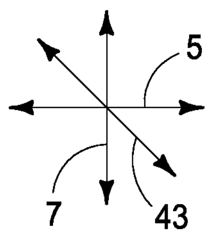
FIG. 14



Y-Y
FIG. 14B



X-X
FIG. 14A



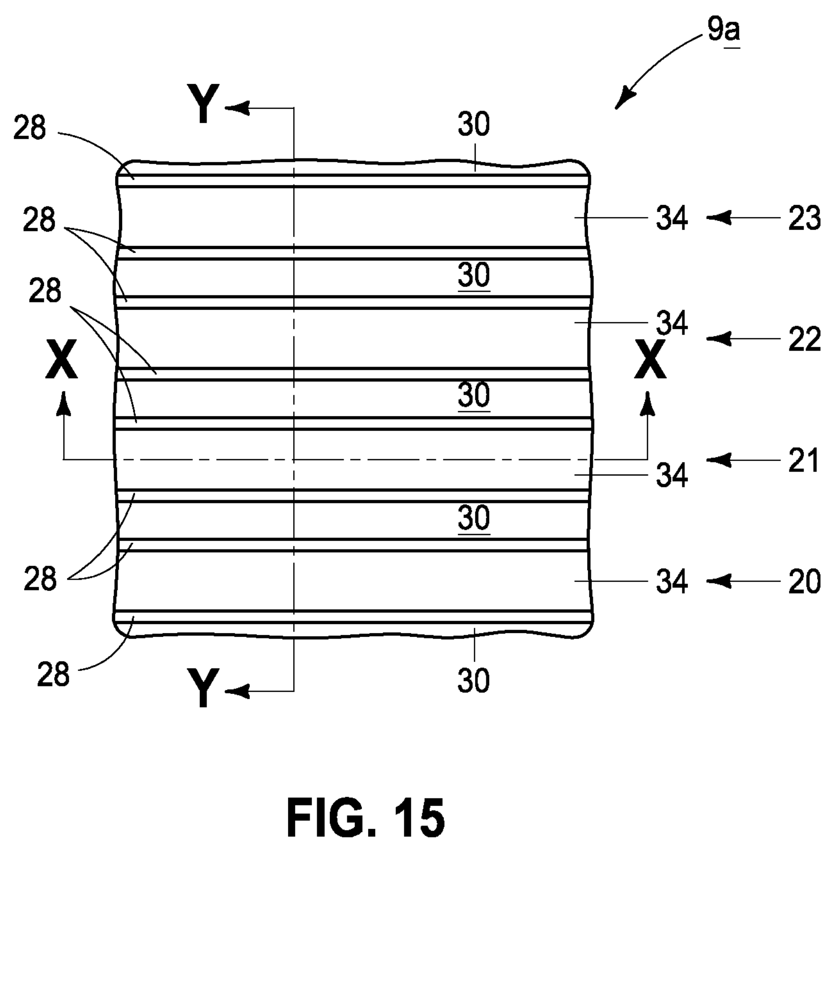
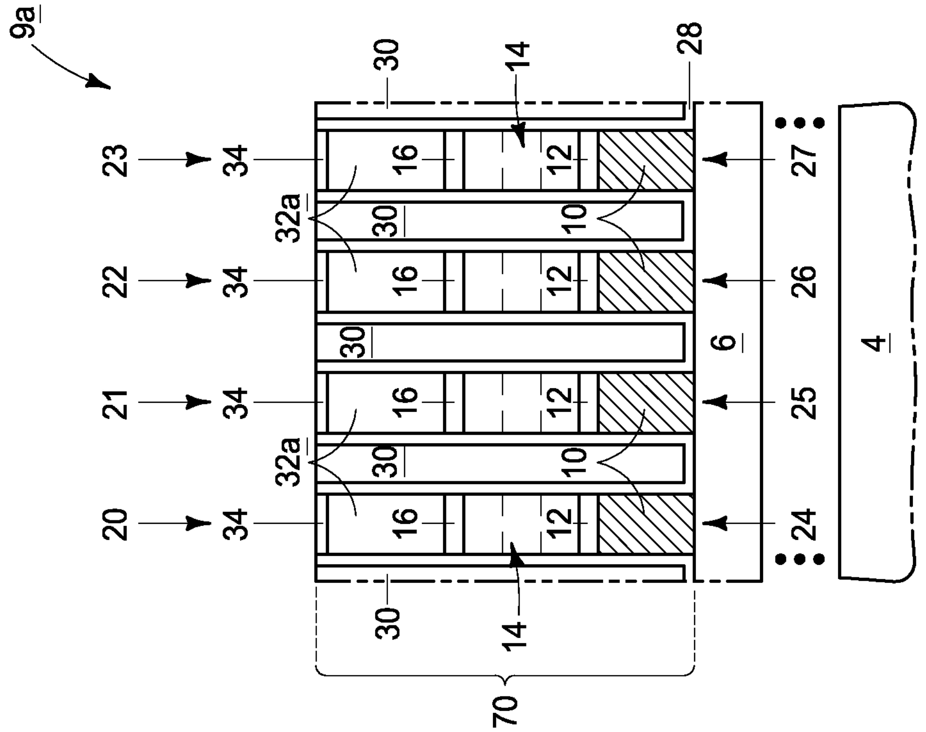
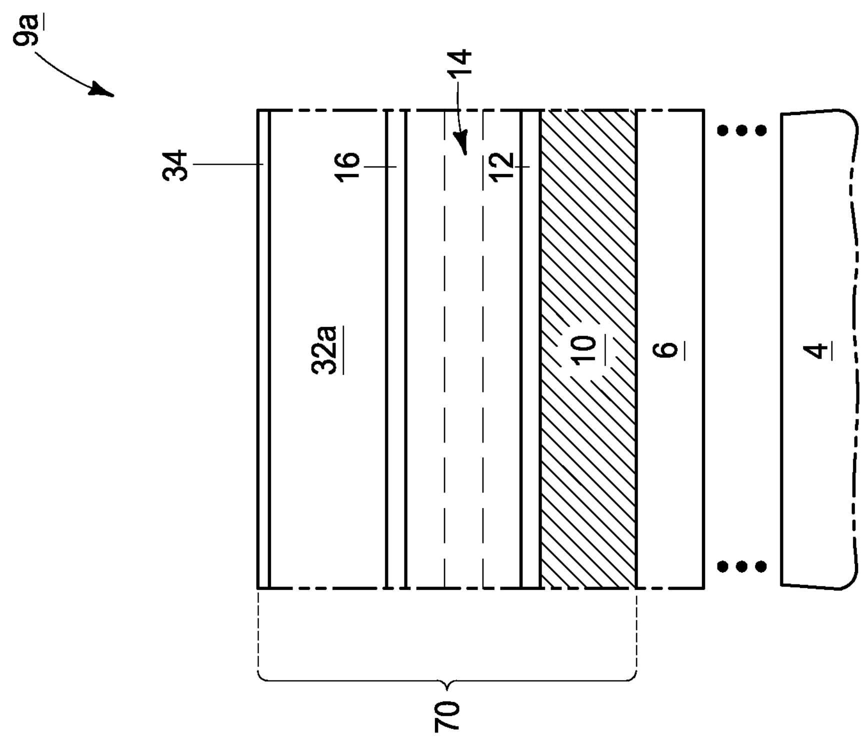


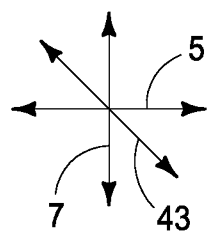
FIG. 15



Y-Y
FIG. 15B



X-X
FIG. 15A



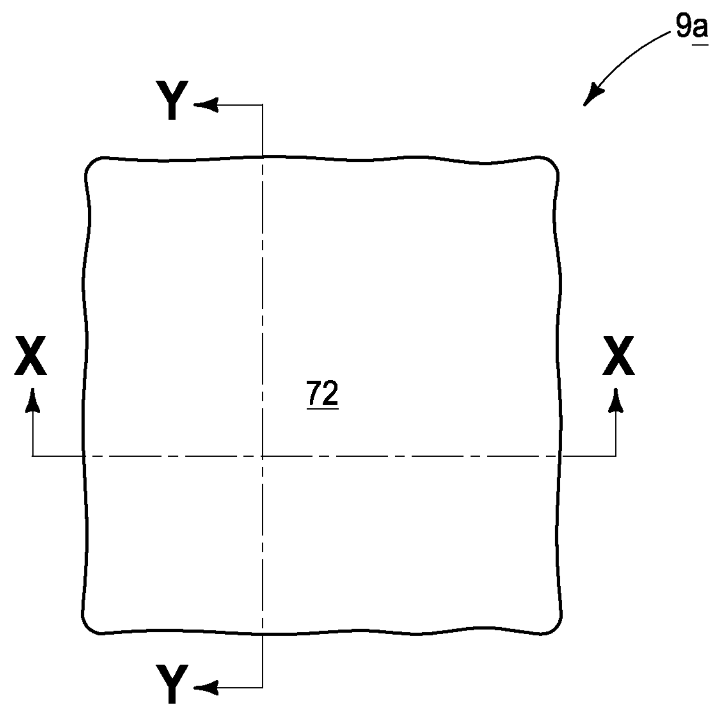
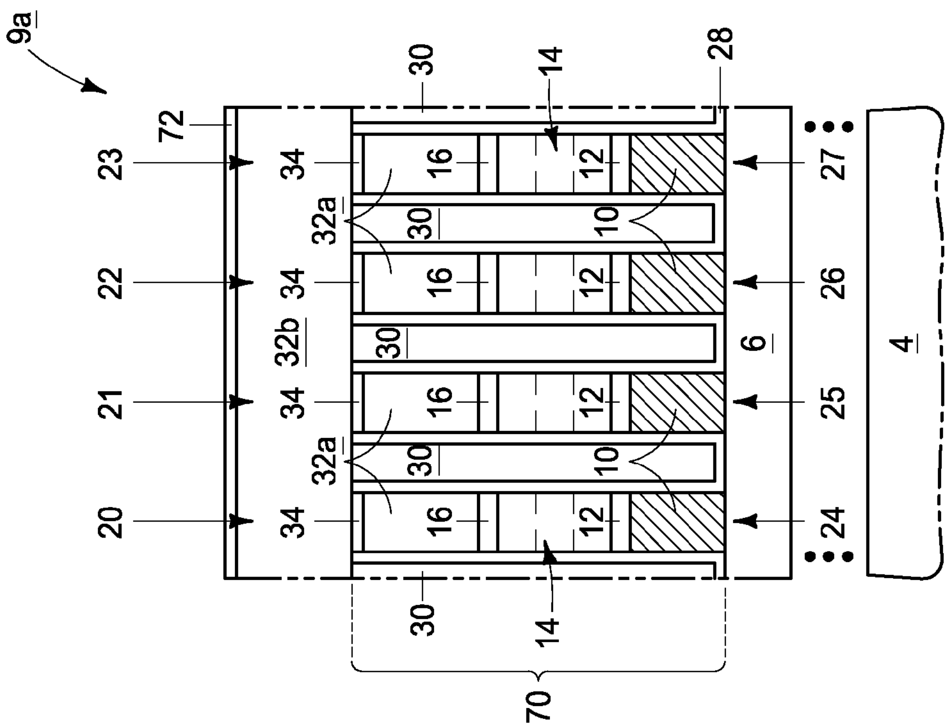
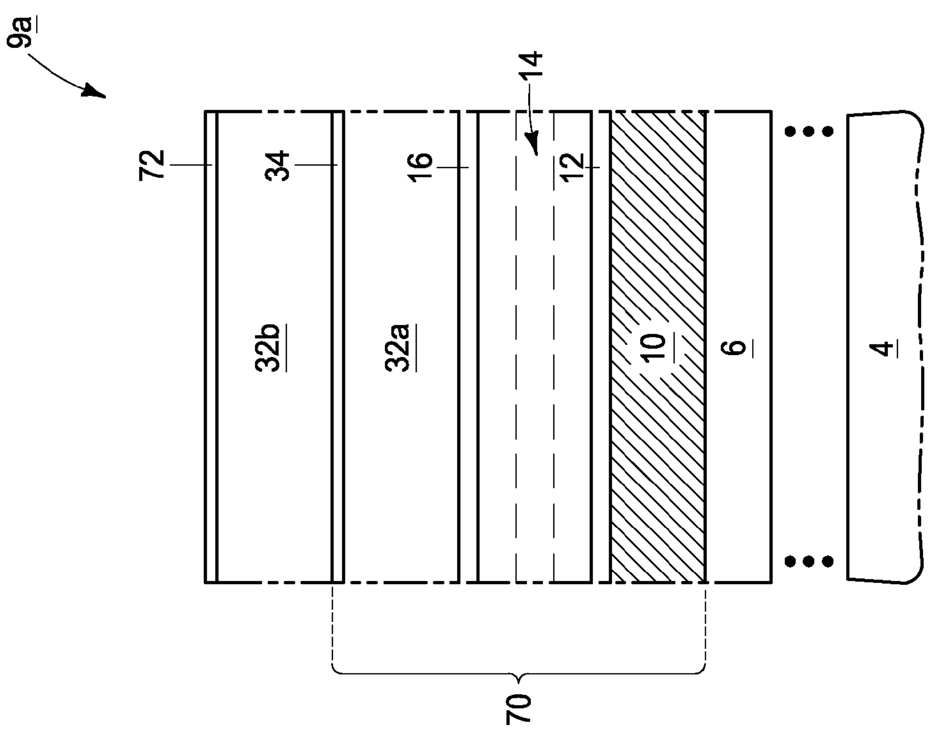


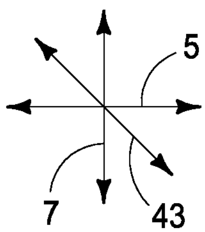
FIG. 16



Y-Y
FIG. 16B



X-X
FIG. 16A



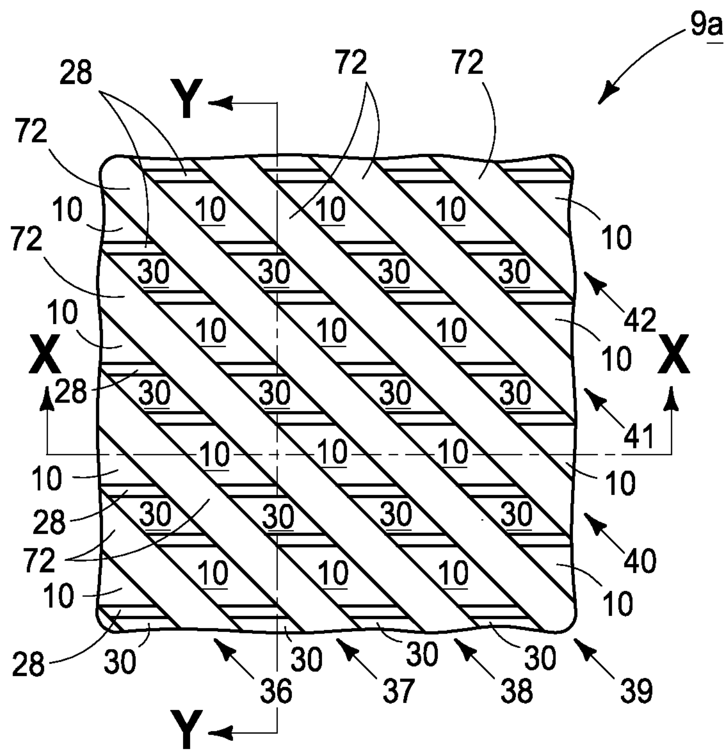
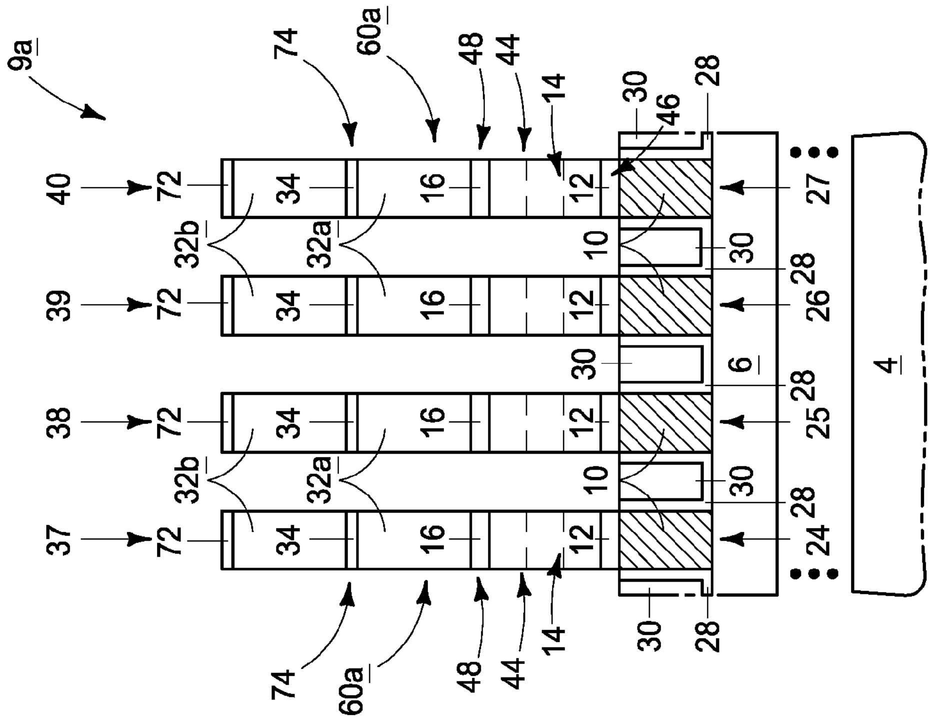
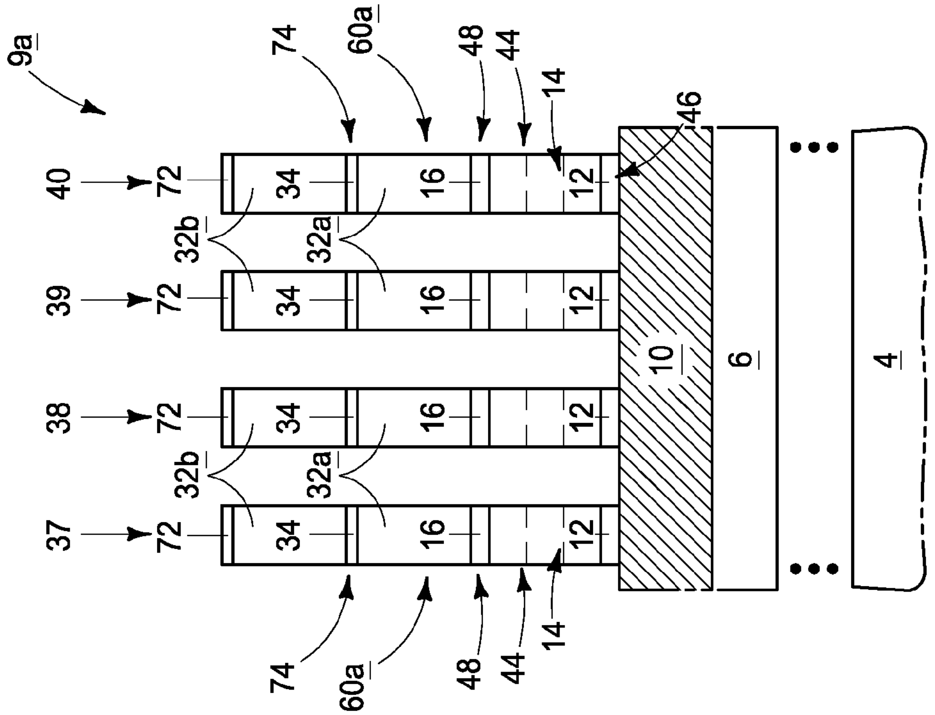


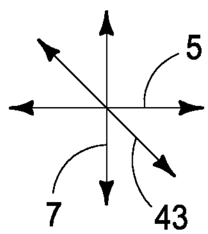
FIG. 17



Y-Y
FIG. 17B



X-X
FIG. 17A



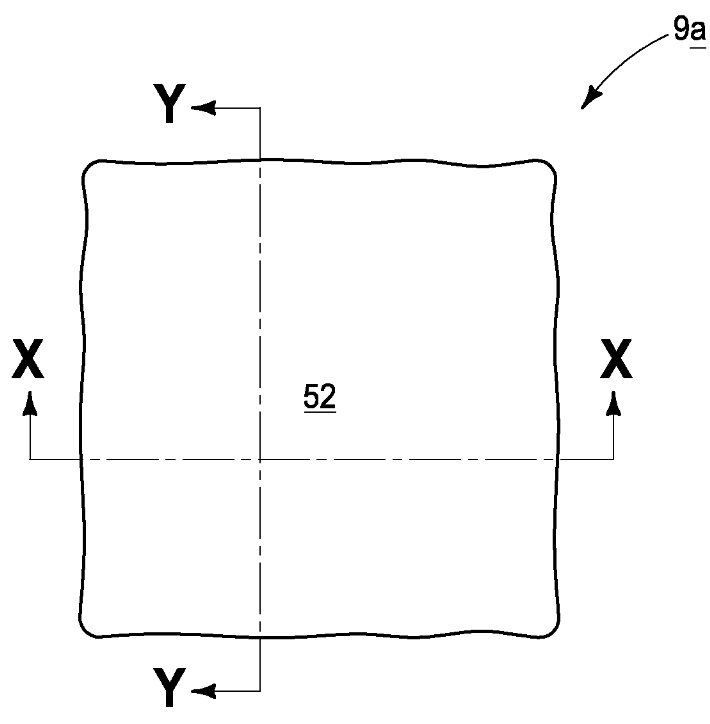
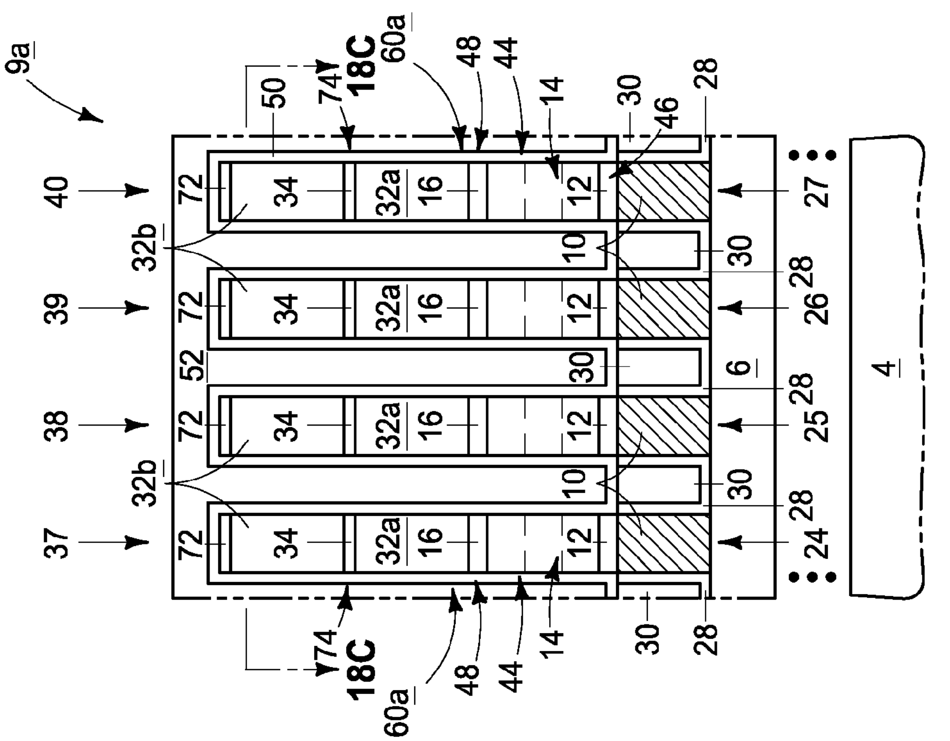
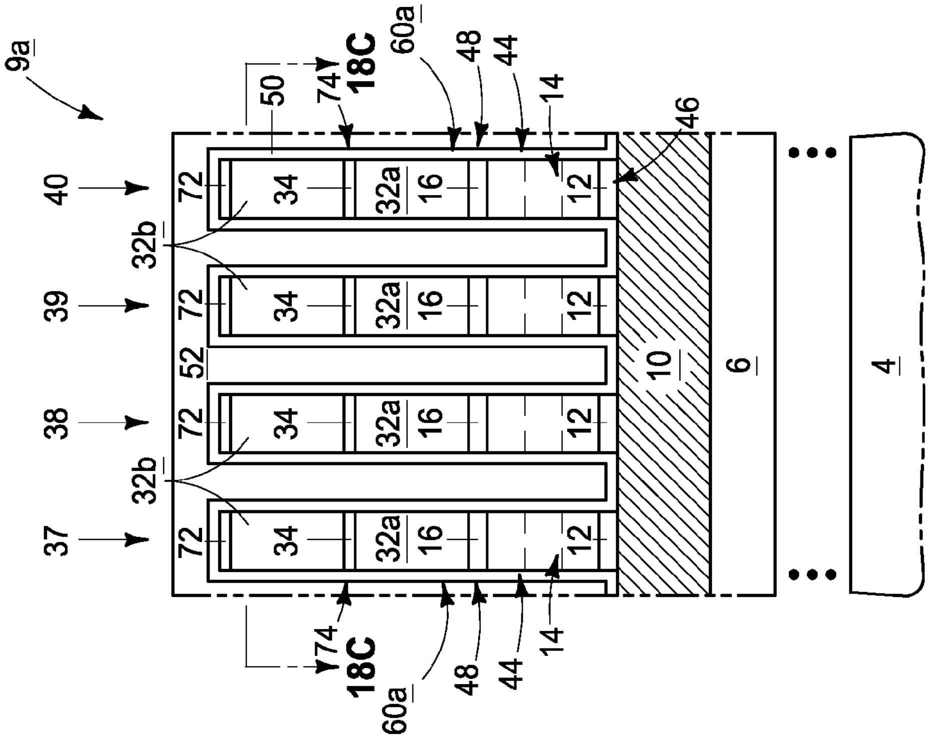


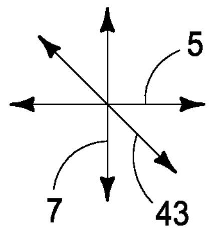
FIG. 18



Y-Y
FIG. 18B



X-X
FIG. 18A


5
7
43

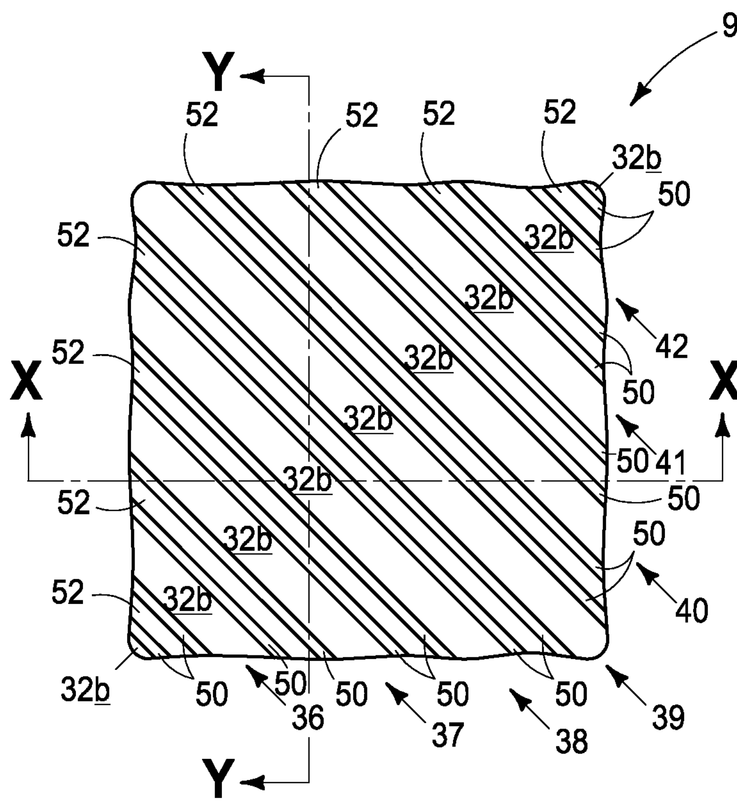
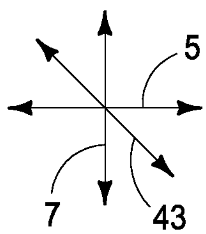

9a
Y
Y
X
X
52
52
52
52
32b
50
32b
32b
32b
32b
32b
32b
32b
42
41
40
39
38
37
36

FIG. 18C



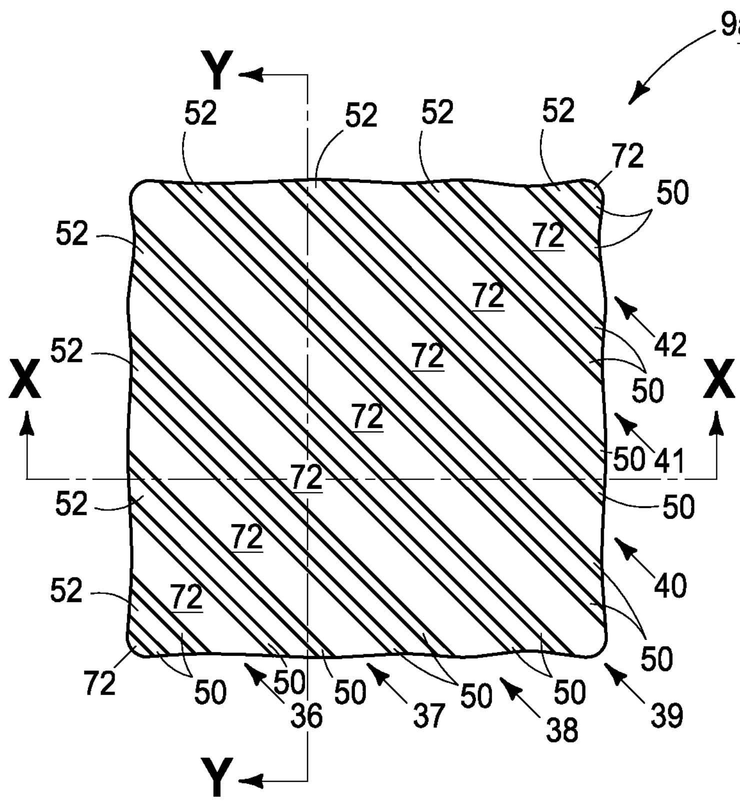
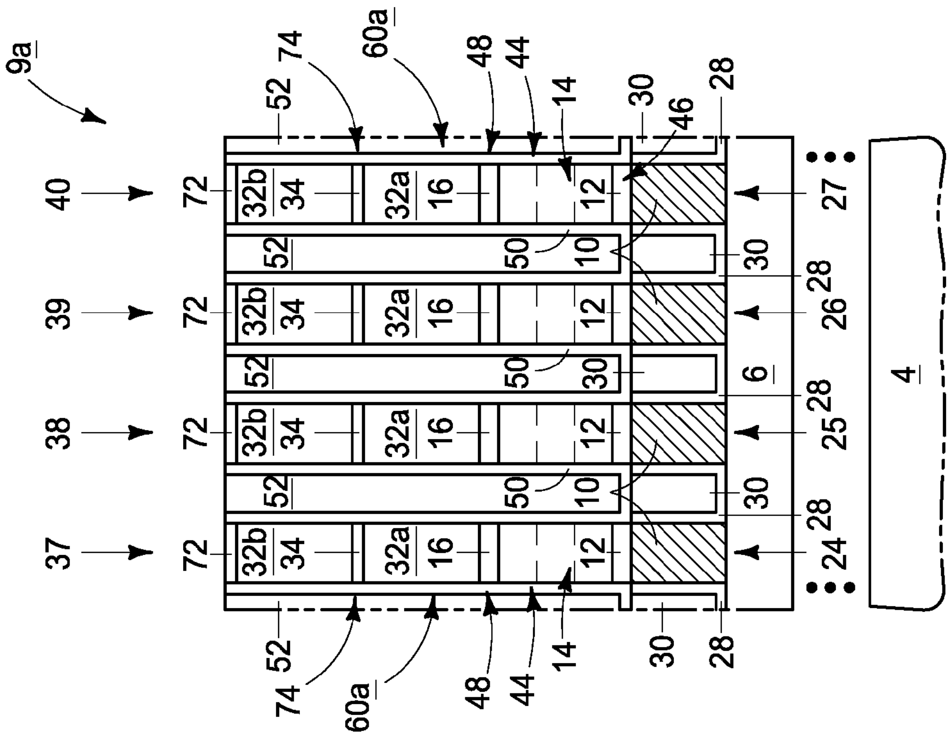
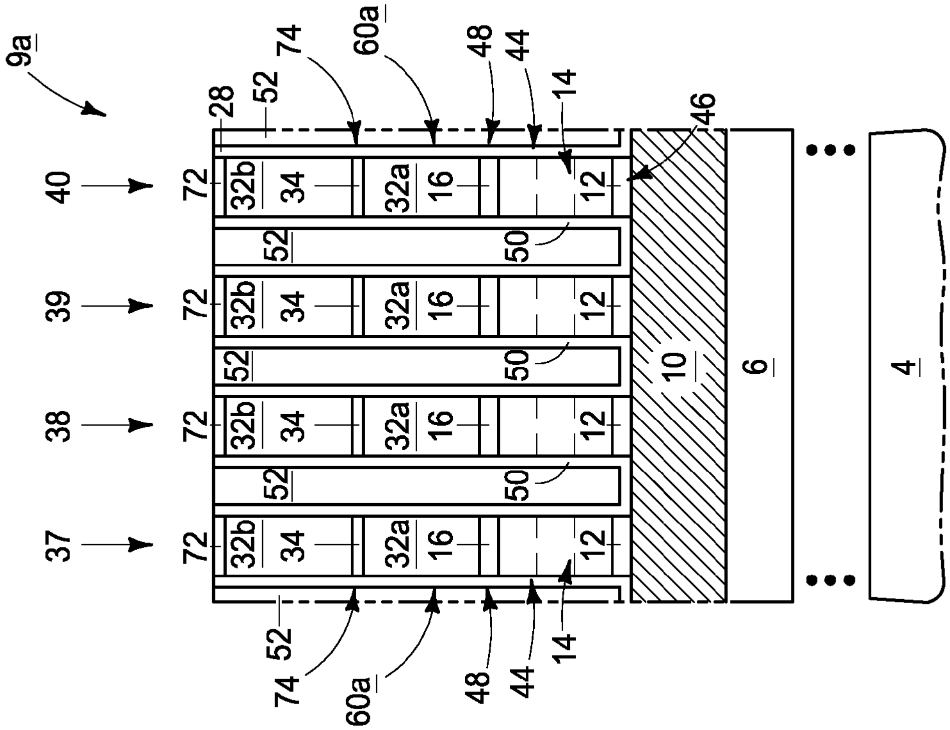


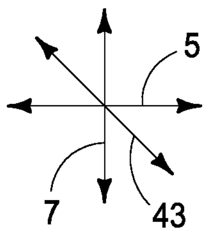
FIG. 19



Y-Y
FIG. 19B



X-X
FIG. 19A



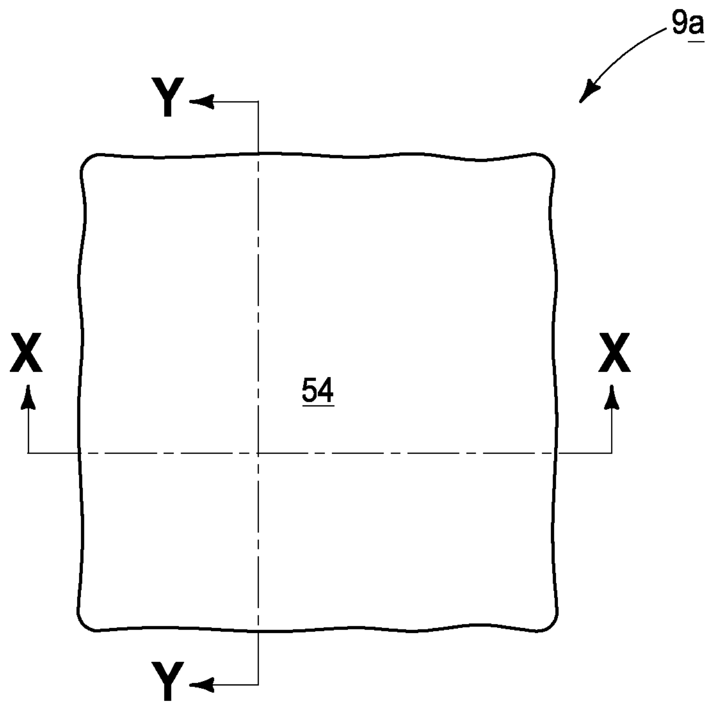
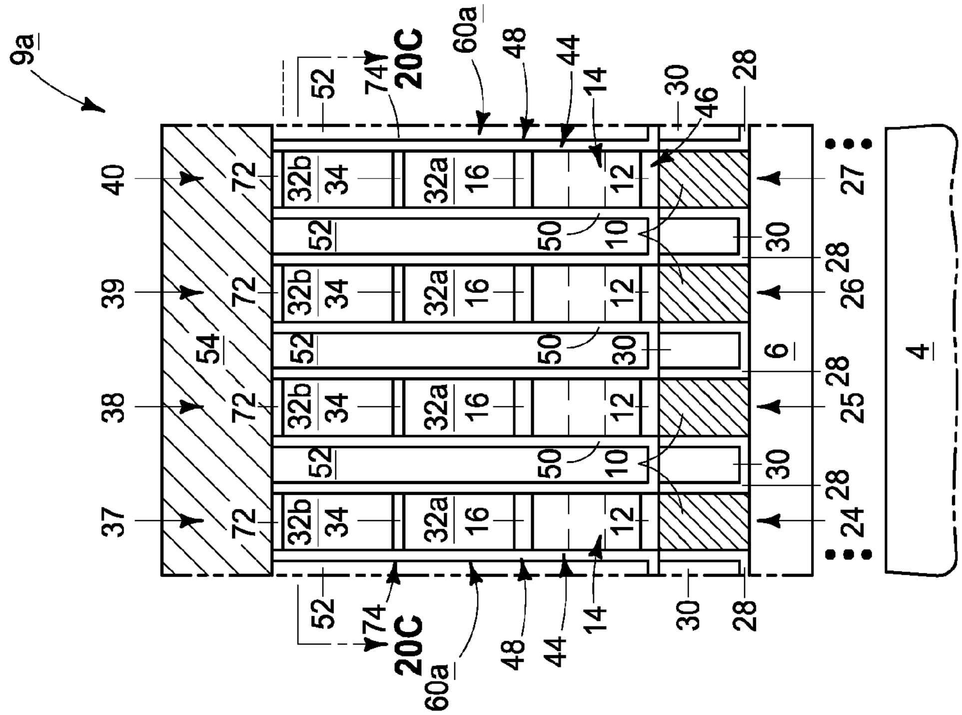
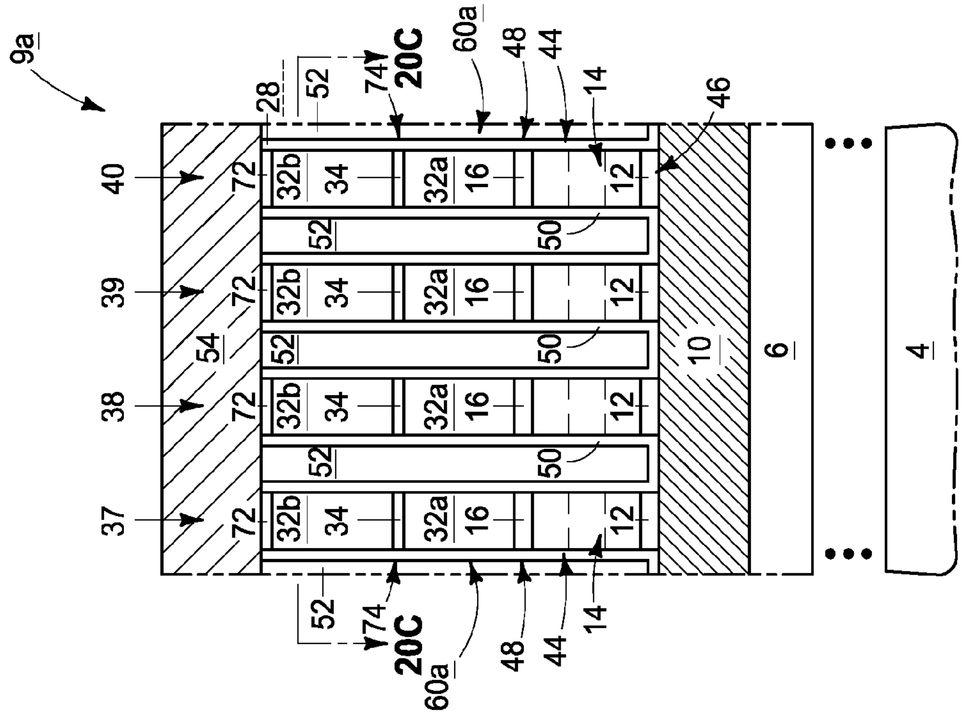


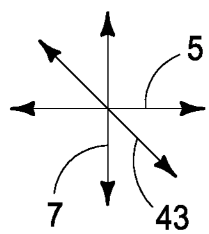
FIG. 20



Y-Y
FIG. 20B



X-X
FIG. 20A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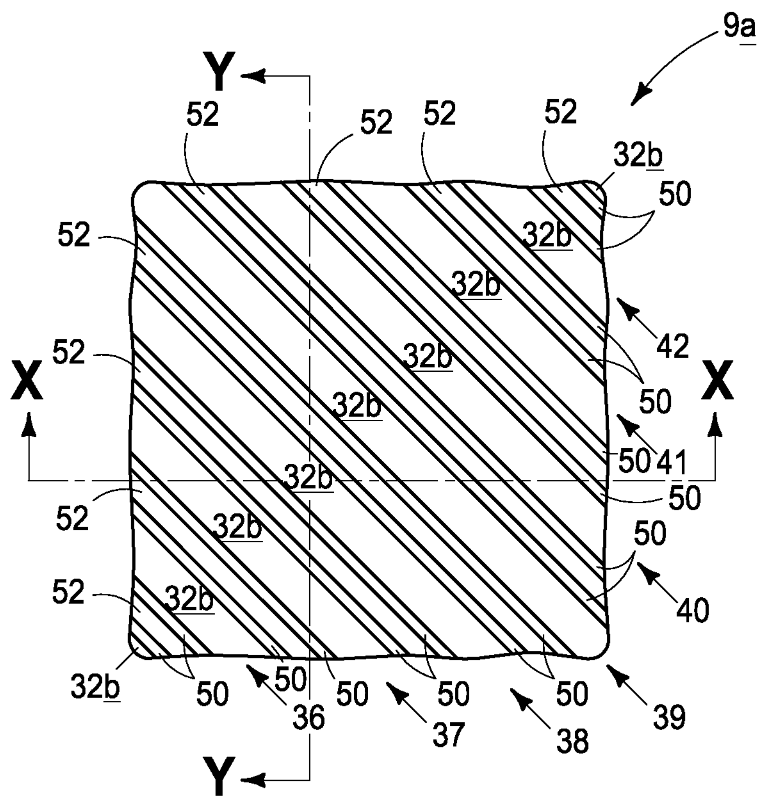
7
43


9a
Y
52
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52
52
32b
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32b
32b
32b
32b
32b
32b
32b
X
X
42
50
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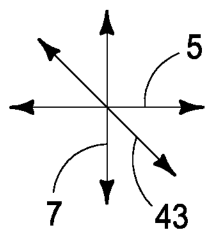
41
50
50
40
39
38
37
36
50
50
50
50
50
32b
Y

FIG. 20C



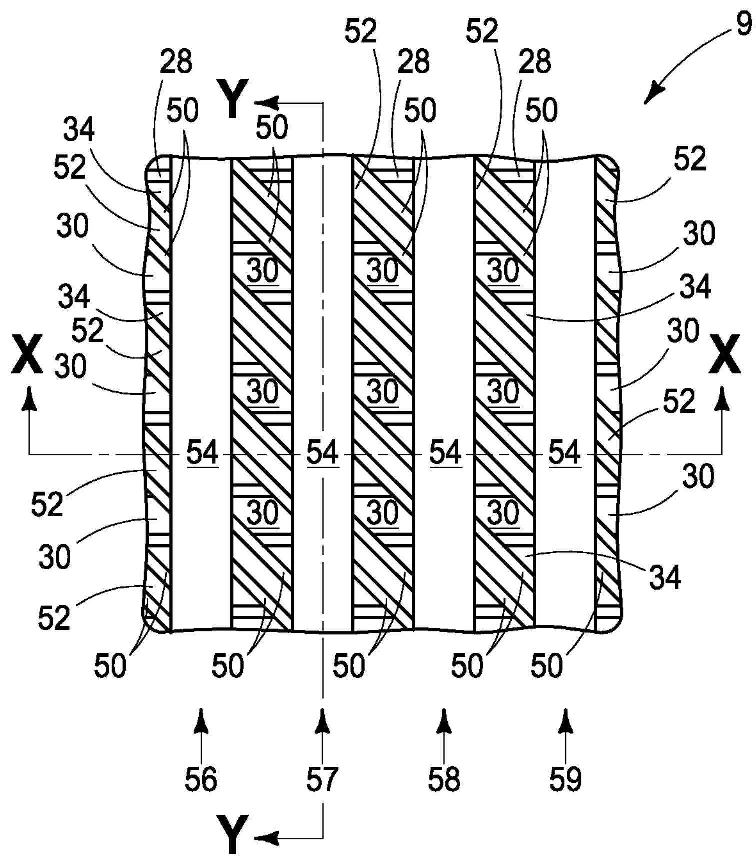
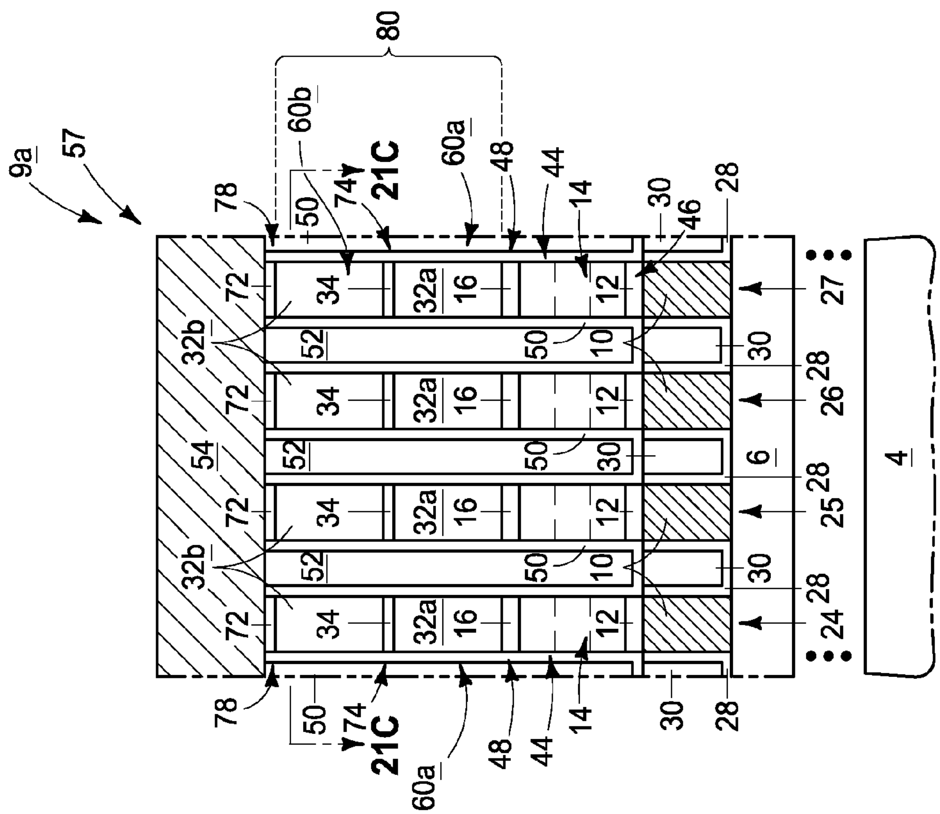
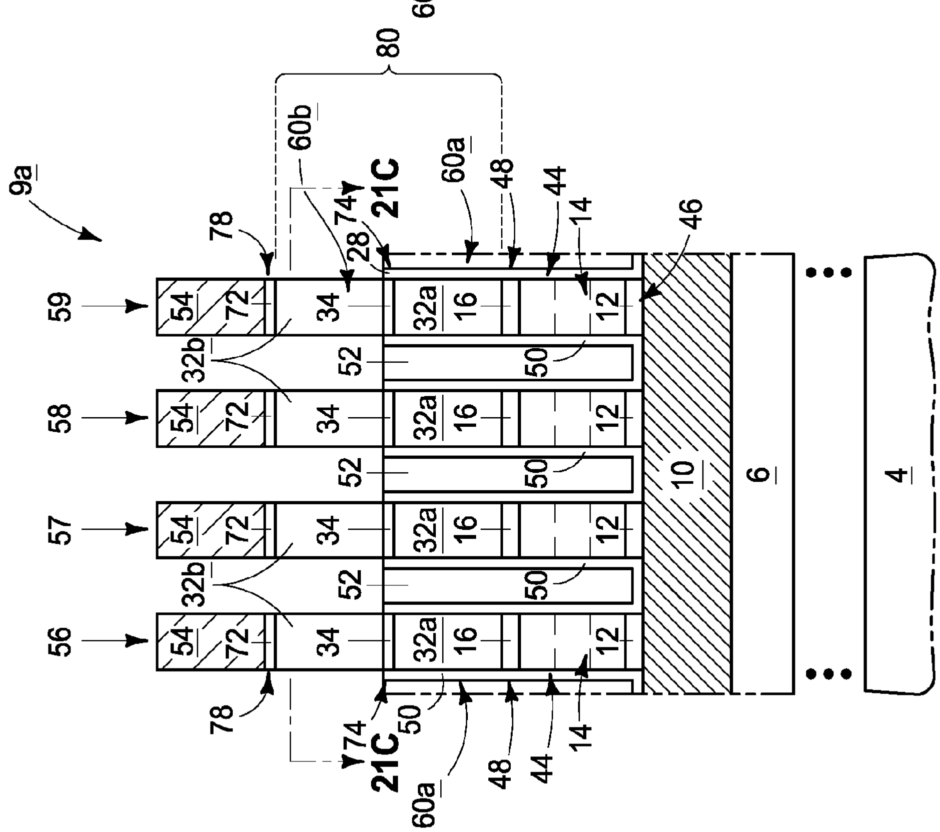


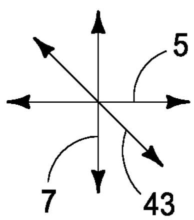
FIG. 21



Y-Y
FIG. 21B



X-X
FIG. 21A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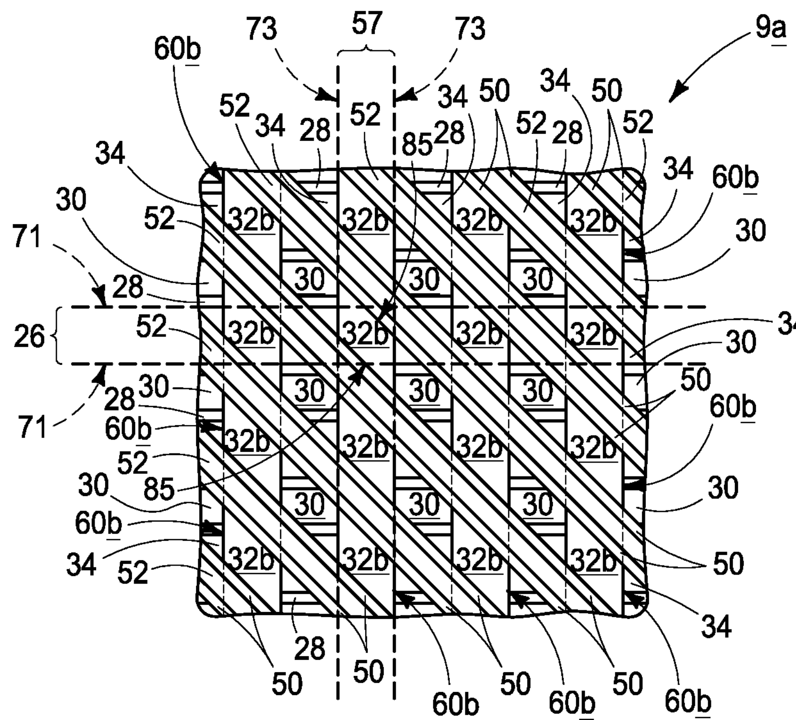
7
43


73
57
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9a
60b
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85
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32b
30
71
26
52
28
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60b
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60b
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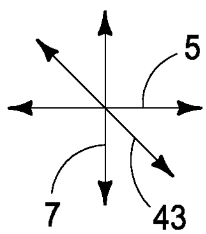
50
60b
50
60b
50
60b

FIG. 21C



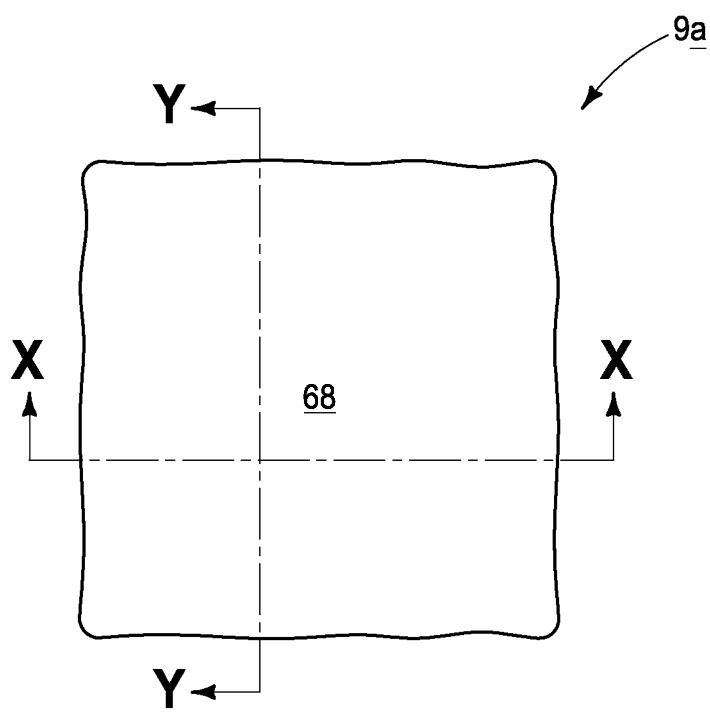
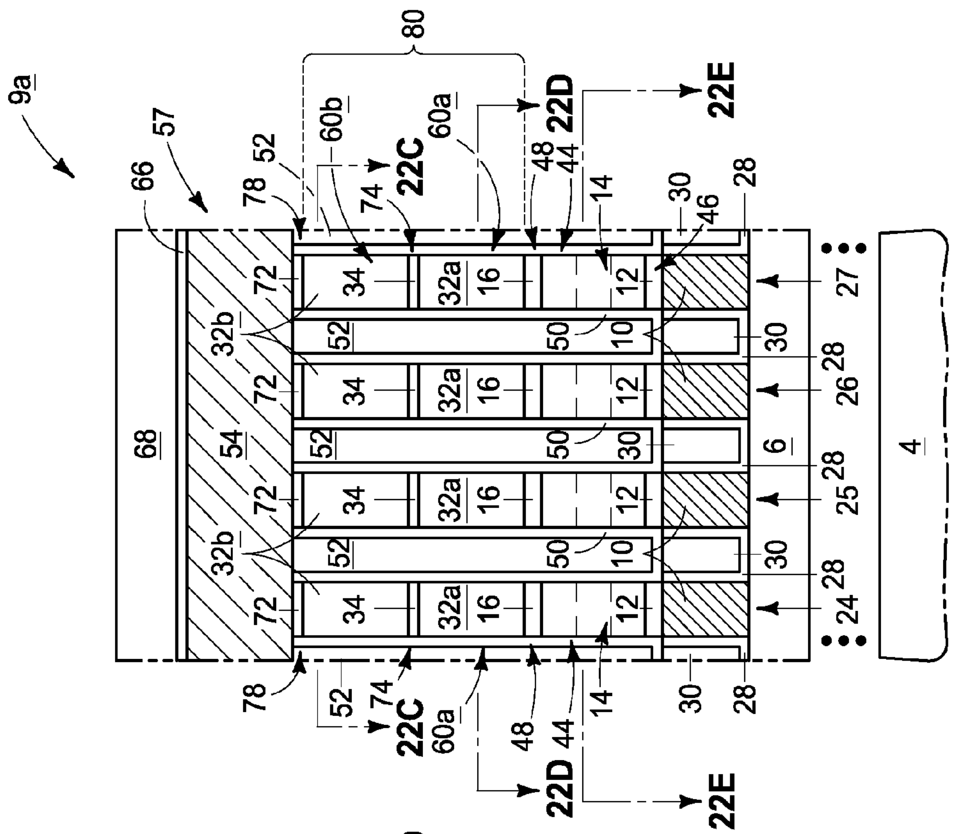
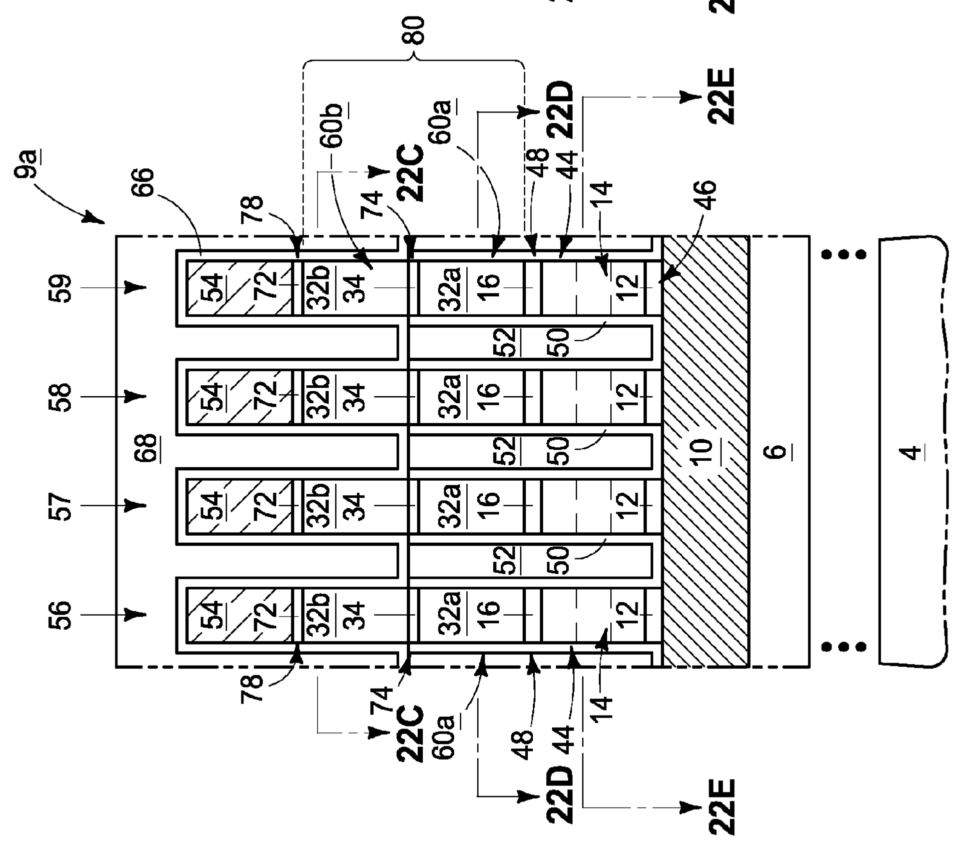


FIG. 22



Y-Y
FIG. 22B



X-X
FIG. 22A

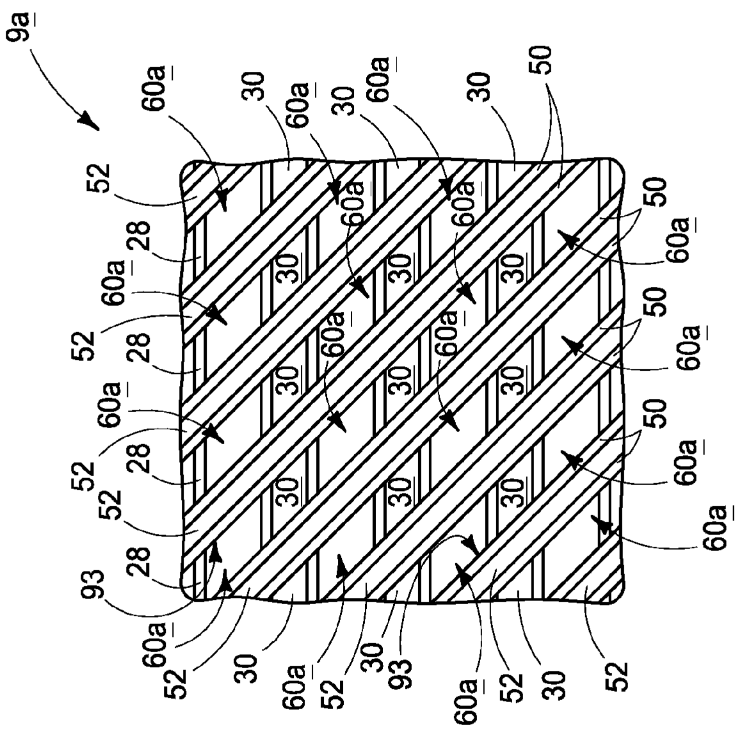


FIG. 22D

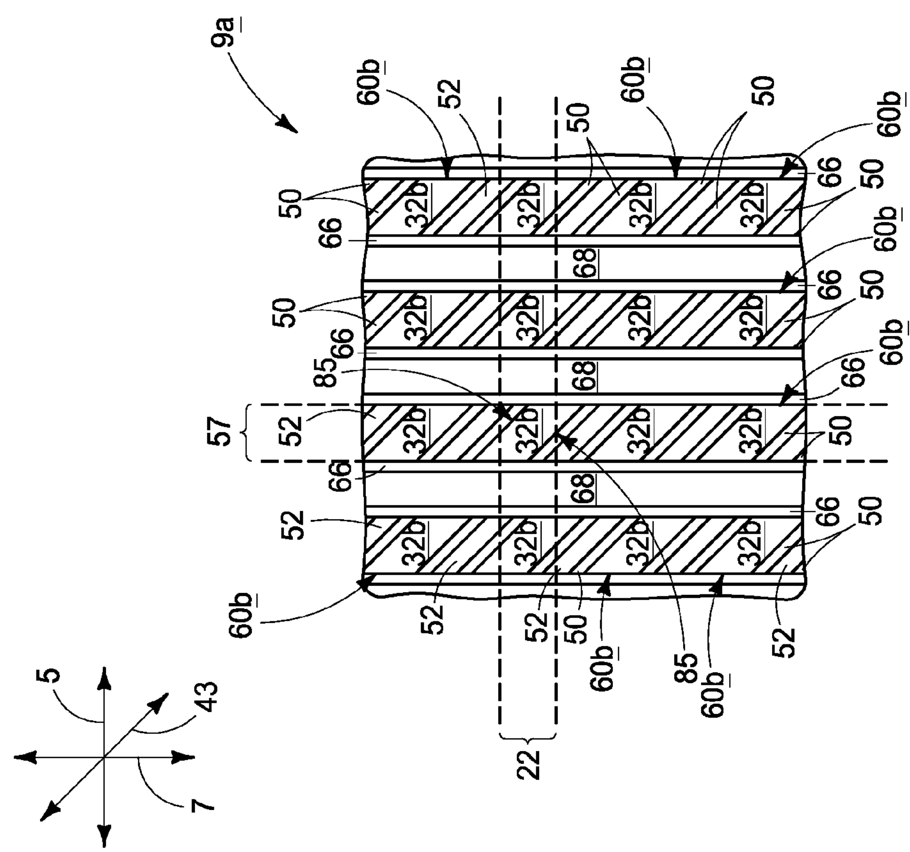


FIG. 22C

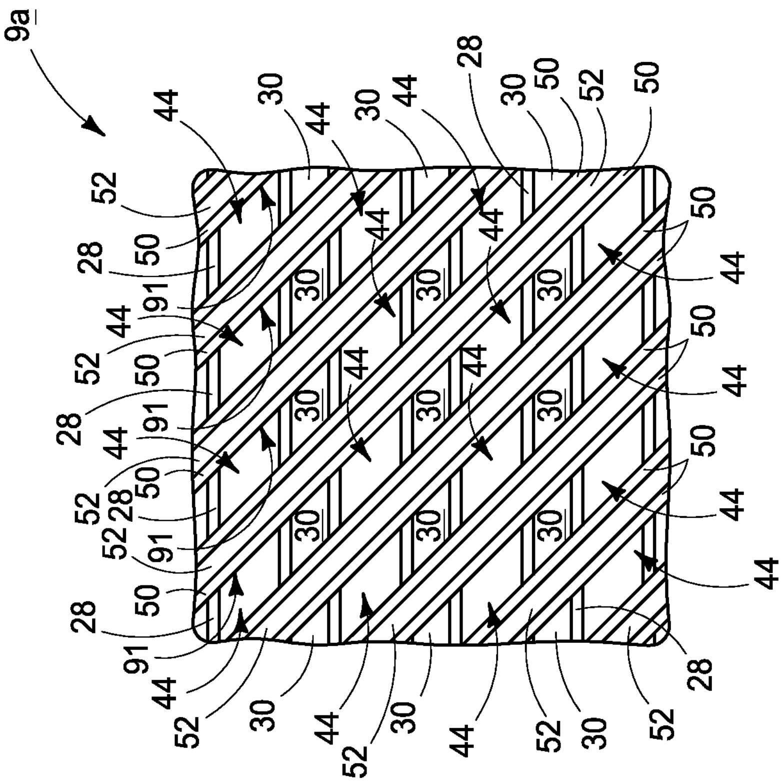
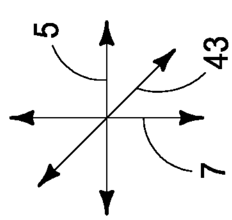


FIG. 22E



MEMORY ARRAYS WITH POLYGONAL MEMORY CELLS HAVING SPECIFIC SIDEWALL ORIENTATIONS

TECHNICAL FIELD

Memory arrays and methods of forming memory arrays.

BACKGROUND

Memory is one type of integrated circuitry, and is used in systems for storing data. Memory is usually fabricated in one or more arrays of individual memory cells. The memory cells are configured to retain or store information in at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store more than two levels or states of information.

Integrated circuit fabrication continues to strive to produce smaller and denser integrated circuits. Accordingly, there has been substantial interest in memory cells that can be utilized in structures having programmable material between a pair of electrodes; where the programmable material has two or more selectable resistive states to enable storing of information. Examples of such memory cells are resistive RAM (RRAM) cells, phase change RAM (PCRAM) cells, and programmable metallization cells (PMCs)—which may be alternatively referred to as a conductive bridging RAM (CBRAM) cells, nanobridge memory cells, or electrolyte memory cells. The memory cell types are not mutually exclusive. For example, RRAM may be considered to encompass PCRAM and PMCs. Additional example memory includes ferroelectric memory, magnetic RAM (MRAM) and spin-torque RAM.

It would be desirable to develop improved memory arrays, and improved methods of forming memory arrays.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1-1**B are a top view and cross-sectional side views of a region of a semiconductor construction at a processing stage of an example embodiment method of forming a memory array. The views of FIGS. **1**A and **1**B are along the lines X-X and Y-Y of FIG. **1**, respectively.

FIGS. **2-2**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **1-1**B. The views of FIGS. **2**A and **2**B are along the lines X-X and Y-Y of FIG. **2**, respectively.

FIGS. **3-3**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **2-2**B. The views of FIGS. **3**A and **3**B are along the lines X-X and Y-Y of FIG. **3**, respectively.

FIGS. **4-4**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **3-3**B. The views of FIGS. **4**A and **4**B are along the lines X-X and Y-Y of FIG. **4**, respectively.

FIGS. **5-5**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **4-4**B. The views of FIGS. **5**A and **5**B are along the lines X-X and Y-Y of FIG. **5**, respectively.

FIGS. **6-6**C are a top view, cross-sectional side views, and a cross-sectional plan view of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **5-5**B. The cross-sectional side views of FIGS. **6**A and **6**B are along the lines X-X and Y-Y of FIG. **6**, respectively; and the cross-sectional plan view of FIG. **6**C is along the lines **6**C-**6**C of FIGS. **6**A and **6**B.

FIGS. **7-7**D are a top view, cross-sectional side views, and cross-sectional plan views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **6-6**C. The cross-sectional side views of FIGS. **7**A and **7**B are along the lines X-X and Y-Y of FIG. **7**, respectively; and the cross-sectional plan views of FIGS. **7**C and **7**D are along the lines **7**C-**7**C and **7**D-**7**D of FIGS. **7**A and **7**B.

FIGS. **8-8**C are a top view, cross-sectional side views, and a cross-sectional plan view of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **7-7**D. The cross-sectional side views of FIGS. **8**A and **8**B are along the lines X-X and Y-Y of FIG. **8**, respectively; and the cross-sectional plan view of FIG. **8**C is along the lines **8**C-**8**C of FIGS. **8**A and **8**B.

FIGS. **9-9**D are a top view, cross-sectional side views, and cross-sectional plan views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **8-8**C. The cross-sectional side views of FIGS. **9**A and **9**B are along the lines X-X and Y-Y of FIG. **9**, respectively; and the cross-sectional plan views of FIGS. **9**C and **9**D are along the lines **9**C-**9**C and **9**D-**9**D of FIGS. **9**A and **9**B.

FIGS. **10-10**D are a top view, cross-sectional side views, and cross-sectional plan views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **9-9**D. The cross-sectional side views of FIGS. **10**A and **10**B are along the lines X-X and Y-Y of FIG. **10**, respectively; and the cross-sectional plan views of FIGS. **10**C and **10**D are along the lines **10**C-**10**C and **10**D-**10**D of FIGS. **10**A and **10**B.

FIGS. **11-11**D are a top view, cross-sectional side views, and cross-sectional plan views of the semiconductor construction of FIGS. **1-1**B at a processing stage subsequent to that of FIGS. **10-10**D. The cross-sectional side views of FIGS. **11**A and **11**B are along the lines X-X and Y-Y of FIG. **11**, respectively; and the cross-sectional plan views of FIGS. **11**C and **11**D are along the lines **11**C-**11**C and **11**D-**11**D of FIGS. **11**A and **11**B.

FIGS. **12-12**B are a top view and cross-sectional side views of a region of a semiconductor construction at a processing stage of another example embodiment method of forming a memory array. The views of FIGS. **12**A and **12**B are along the lines X-X and Y-Y of FIG. **12**, respectively.

FIGS. **13-13**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **12-12**B. The views of FIGS. **13**A and **13**B are along the lines X-X and Y-Y of FIG. **13**, respectively.

FIGS. **14-14**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **13-13**B. The views of FIGS. **14**A and **14**B are along the lines X-X and Y-Y of FIG. **14**, respectively.

FIGS. **15-15**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **14-14**B. The views of FIGS. **15**A and **15**B are along the lines X-X and Y-Y of FIG. **15**, respectively.

FIGS. **16-16**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **15-15**B. The views of FIGS. **16**A and **16**B are along the lines X-X and Y-Y of FIG. **16**, respectively.

FIGS. **17-17**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **16-16**B. The views of FIGS. **17**A and **17**B are along the lines X-X and Y-Y of FIG. **17**, respectively.

FIGS. **18-18**C are a top view, cross-sectional side views, and a cross-sectional plan view of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **17-17**B. The cross-sectional side views of FIGS. **18**A and **18**B are along the lines X-X and Y-Y of FIG. **18**, respectively; and the cross-sectional plan view of FIG. **18**C is along the lines **18**C-**18**C of FIGS. **18**A and **18**B.

FIGS. **19-19**B are a top view and cross-sectional side views of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **18-18**C. The views of FIGS. **19**A and **19**B are along the lines X-X and Y-Y of FIG. **19**, respectively.

FIGS. **20-20**C are a top view, cross-sectional side views, and a cross-sectional plan view of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **19-19**B. The cross-sectional side views of FIGS. **20**A and **20**B are along the lines X-X and Y-Y of FIG. **20**, respectively; and the cross-sectional plan view of FIG. **20**C is along the lines **20**C-**20**C of FIGS. **20**A and **20**B.

FIGS. **21-21**C are a top view, cross-sectional side views, and a cross-sectional plan view of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **20-20**C. The cross-sectional side views of FIGS. **21**A and **21**B are along the lines X-X and Y-Y of FIG. **21**, respectively; and the cross-sectional plan view of FIG. **21**C is along the lines **21**C-**21**C of FIGS. **21**A and **21**B.

FIGS. **22-22**E are a top view, cross-sectional side views, and cross-sectional plan views of the semiconductor construction of FIGS. **12-12**B at a processing stage subsequent to that of FIGS. **21-21**C. The cross-sectional side views of FIGS. **22**A and **22**B are along the lines X-X and Y-Y of FIG. **22**, respectively; and the cross-sectional plan views of FIGS. **22**C, **22**D and **22**E are along the lines **22**C-**22**C, **22**D-**22**D and **22**E-**22**E of FIGS. **22**A and **22**B.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

In some embodiments, the invention includes memory arrays in which memory cells are provided within pillars between lower access/sense lines and upper access/sense lines, and in which upper portions of the pillars have different peripheral configurations than lower portions of the pillars. Such configurations may improve structural integrity of the pillars relative to conventional configurations. Some embodiments include new methods of forming memory arrays. Example embodiments are described below with reference to FIGS. **1-22**.

Referring to FIGS. **1-1**B, a portion of a construction **9** is illustrated at a processing stage of an example embodiment method for fabricating an example embodiment memory array.

The construction **9** comprises a semiconductor base **4**, and an electrically insulative material **6** supported over the base **4**. The insulative material **6** is shown spaced from the base **4** to indicate that there may be one or more other materials and/or integrated circuit levels between the base **4** and the insulative material **6**.

The base **4** may comprise semiconductor material; and may, for example, comprise, consist essentially of, or consist of monocrystalline silicon. In some embodiments, base **4** may be considered to comprise a semiconductor substrate. The term "semiconductor substrate" means any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductor substrates described above. In some embodiments, base **4** may correspond to a semiconductor substrate containing one or more materials associated with integrated circuit fabrication. Some of the materials may be between the shown region of base **4** and the insulative material **6** and/or may be laterally adjacent the shown region of base **4**; and may correspond to, for example, one or more of refractory metal materials, barrier materials, diffusion materials, insulator materials, etc.

The insulative material **6** may comprise any suitable composition or combination of compositions; including, for example, one or more of various oxides (for instance, silicon dioxide, borophosphosilicate glass, etc.), silicon nitride, etc.

A stack **8** of materials is formed over the insulative material **6**. Such stack includes access/sense material **10**, first electrode material **12**, one or more select device materials **14**, and second electrode material **16**.

The access/sense material **10** is electrically conductive and may comprise any suitable composition or combination of compositions. In some embodiments, material **10** may comprise, consist essentially of, or consist of one or more of various metals (for example, tungsten, titanium, etc.), metal-containing compositions (for instance, metal nitride, metal carbide, metal silicide, etc.), and conductively-doped semiconductor materials (for instance, conductively-doped silicon, conductively-doped germanium, etc.). In some embodiments, the access/sense material **10** may be referred to as a first access/sense material to distinguish it from other access/sense materials formed later.

The electrode materials **12** and **16** may comprise any suitable compositions or combinations of compositions; and in some embodiments may comprise, consist essentially of, or consist of carbon. The electrode materials **12** and **16** may be the same as one another in some embodiments, and may differ from one another in other embodiments.

The select device material is ultimately utilized to form select devices suitable for utilization in a memory array. The select devices may be any suitable devices; including, for example, diodes, bipolar junction transistors, field effect transistors, switches, etc. Different materials of the select devices are diagrammatically illustrated in FIGS. **1**A and **1**B using dashed lines to indicate approximate boundaries between various materials of example devices, and using label **14** to refer generally to all of the various materials of the select devices.

Referring to FIGS. **2-2**B, stack **8** is patterned into lines **20-23** extending along the direction of an axis **5**. Such direction may be referred to as a first direction in the discussion that follows, and is orthogonal to a second direction designated by an axis **7**. The lines **20-23** are on a pitch "P". Such pitch may comprise any suitable dimension, and in some embodiments may be within a range of from about 40 nm to about 200 nm.

The lines **20-23** may be formed with any suitable processing. For instance, a patterned mask (not shown) may be formed over stack **8**, a pattern may be transferred from the mask into the materials of stack **8** with one or more suitable etches, and then the mask may be removed to leave the construction of FIGS. **2-2**B. The mask may be a lithographic mask (for instance, a photolithographically-patterned photoresist mask) or a sublithographic mask (for instance, a mask formed utilizing pitch-multiplication methodologies).

The patterned access/sense material **10** forms a series of access/sense lines **24-27**. In some embodiments, the lines **24-27** may be referred to as first access/sense lines to distinguish them from other access/sense lines formed later.

Referring to FIGS. **3-3**B, insulative materials **28** and **30** are formed over and between the lines **20-23**. The materials **28** and **30** may comprise any suitable electrically insulative compositions, or combinations of compositions. In some embodiments, insulative material **28** may comprise, consist essentially of, or consist of silicon nitride; and insulative material **30** may comprise, consist essentially of, or consist of silicon dioxide. Although two insulative materials (**28** and **30**) are shown, in other embodiments only a single insulative material may be formed over and between the lines **20-23**, and in yet other embodiments more than two insulative materials may be formed over and between the lines **20-23**.

Referring to FIGS. **4-4**B, the insulative materials **28** and **30** are removed from over lines **20-23**, which exposes a surface of the second electrode material **16** at the tops of the lines. In some embodiments, the materials **28** and **30** may be removed utilizing planarization, such as, for example, chemical-mechanical polishing (CMP).

Referring to FIGS. **5-5**B, programmable material **32** is formed across lines **20-23**; and in the shown embodiment is formed over and directly against the exposed upper surfaces of electrode material **16**.

The programmable material may comprise any suitable composition. In some embodiments, the programmable material may comprise a phase change material, such as a chalcogenide. For example, the programmable material may comprise germanium, antimony and tellurium; and may correspond to a chalcogenide commonly referred to as GST. In other example embodiments, the programmable material may comprise other compositions suitable for utilization in other types of memory besides phase change memory. For instance, the programmable material may comprise one or more compositions suitable for utilization in CBRAM or other types of resistive RAM.

The programmable material may be formed to any suitable thickness, and in some embodiments may be formed to a vertical thickness of at least about 60 nm; such as, for example, a vertical thickness of from about 60 nm to about 100 nm. Such thicknesses may be significantly greater than conventional thicknesses of programmable material. Ultimately, the programmable material is incorporated into pillars (for instance, pillars described below with reference to FIGS. **10-10**D). Conventional processing utilizes two crossing patterns to pattern the programmable material to have a simple square or rectangular peripheral shape. In embodiments described herein, an additional crossing pattern is utilized so that at least some of the programmable material within the pillars has a different peripheral shape than a simple rectangle or square, which can improve structural integrity of the pillars and thereby enable thicker programmable material to be utilized. The improved structure integrity may enable the pillars to be less susceptible to tipping and/or other structural problems. The greater thickness of the programmable material may enable memory cells to be formed having desired rapid switching characteristics while also having improved separation between different memory states (e.g., "SET" and "RESET" memory states) as compared to memory cells having thinner programmable material.

In the shown embodiment, a third electrode material **34** is formed over programmable material **32**. The third electrode material may comprise any suitable composition or combination of compositions; and in some embodiments may comprise, consist essentially of, or consist of carbon. The third electrode material **34** may be a same composition as one or both of the first and second electrode materials **12** and **16**, or may be a different composition than one or both of electrode materials **12** and **16**.

Referring to FIGS. **6-6**C, the third electrode material **34** and programmable material **32** are patterned into diagonal lines **36-42**. Such diagonal lines cross the first lines **20-23** (FIG. **5**B). The diagonal lines **36-42** extend along a diagonal direction corresponding to an illustrated axis **43**. Such diagonal direction is between the directions of axis **5** and axis **7**, and in some embodiments may be at about 45° relative to the axes **5** and **7**. The diagonal lines are on a pitch P_1. In embodiments in which the diagonal lines extend at 45° relative to the first lines **20-23** (FIG. **4**), the pitch P_1 may be about 0.7P (where P is the pitch of the first lines, as shown in FIG. **2**B). In some embodiments, the first lines of FIGS. **2** and **2**B (lines **20-23**) may be on a different pitch than second lines described below with reference to FIGS. **10** and **10**A (lines **56-59**), and pitch P_1 may be any suitable pitch to achieve stable pillar structures (with example pillar structures being described below with reference to FIGS. **10-10**D). Also, in some embodiments, the first lines of FIGS. **2** and **2**B (lines **20-23**) may be staggered amongst varying pitches rather than all being on the same pitch and/or the second lines of FIGS. **10** and **10**A (lines **56-59**) may be staggered amongst varying pitches rather than all being on the same pitch; and the diagonal lines **36-42** of FIGS. **6-6**C may be staggered amongst varying pitches and/or otherwise may be configured in an appropriate pattern on any pitch or combination of pitches to achieve stable pillar structures.

The diagonal lines **36-42** may be formed with any suitable processing. For instance, a patterned mask (not shown) may be formed over material **34**, a pattern may be transferred from the mask into underlying materials with one or more suitable etches, and then the mask may be removed to leave the construction of FIGS. **6-6**C. The mask may be a lithographic mask (for instance, a photolithographically-patterned photoresist mask) or a sublithographic mask (for instance, a mask formed utilizing pitch-multiplication methodologies).

In the embodiment of FIGS. **6-6**C, a pattern of diagonal lines **36-42** is transferred partially into stack **8** (FIGS. **5**A and **5**B), and specifically is transferred through the first and second electrode materials **12** and **16**, and the select device materials **14**. Such singulates the select device materials into a plurality of select devices **44** as shown along the view of FIG. **6**C; and singulates the first and second electrode materials **12** and **16** into a plurality of first and second electrodes **46** and **48** (only some of which are labeled in the views of FIGS. **6**A and **6**B).

The pattern of diagonal lines **36-42** is also transferred through regions of insulative materials **28** and **30**. Dashed lines **41** (only some of which are labeled) are provided in FIG. **6**C to diagrammatically illustrate that first portions of materials **28** and **30** are raised relative to second portions at the processing stage of FIG. **6**C due to the first portions having been incorporated into diagonal lines **36-42** during etching into materials **28** and **30**.

Referring next to FIGS. **7-7**D, electrically insulative materials **50** and **52** are formed over and between lines **36-42** (FIG. **6**). The insulative materials **50** and **52** may comprise identical compositions as the materials **28** and **30** described above with reference to FIGS. **3-3**B. Accordingly, in some embodiments material **50** may comprise silicon nitride, and material **52** may comprise silicon dioxide. In other embodiments, one or both of materials **50** and **52** may be a different composition than one or both of materials **28** and **30**, and in some embodiments materials **50** and **52** may be replaced with a single material, or may be replaced with more than two materials. In embodiments in which programmable material **32** comprises chalcogenide, it may be advantageous to protect such material from exposure to oxygen. Accordingly, it may be advantageous that material **50** be a non-oxygen-containing material.

Referring to FIGS. **8**-**8**C, the insulative materials **50** and **52** are removed from over lines **36**-**42**, which exposes a surface of the third electrode material **34** at the tops of the lines. In some embodiments, the materials **50** and **52** may be removed utilizing planarization, such as, for example, chemical-mechanical polishing (CMP).

Referring to FIGS. **9**-**9**D, access/sense material **54** is formed across lines **36**-**42**; and in the shown embodiment is formed over and directly against the exposed upper surfaces of electrode material **34**. In some embodiments, the access/sense material **54** may be referred to as a second access/sense material to distinguish it from the first access/sense material **10**.

Referring to FIGS. **10**-**10**D, access/sense material **54** is patterned into access/sense lines **56**-**59** extending along the direction of axis **7**. Accordingly, the lines **56**-**59** may be substantially orthogonal to the lines **20**-**23** (FIGS. **2**-**2**B); with the term "substantially orthogonal" meaning that the lines **56**-**59** are orthogonal to the lines **20**-**23** within reasonable tolerances of fabrication and measurement. The lines **56**-**59** are formed to be on the same pitch "P" as the lines **20**-**23** (FIGS. **2**-**2**B) in the shown embodiment. In other embodiments the lines **56**-**59** may be on a different pitch than the lines **20**-**23**.

The lines **56**-**59** may be formed with any suitable processing. For instance, a patterned mask (not shown) may be formed over material **54**, a pattern may be transferred from the mask into the material **54** with one or more suitable etches, and then the mask may be removed to leave the construction of FIGS. **10**-**10**D. The mask may be a lithographic mask (for instance, a photolithographically-patterned photoresist mask) or a sublithographic mask (for instance, a mask formed utilizing pitch-multiplication methodologies).

The access/sense lines **56**-**59** may be referred to as second access/sense lines to distinguish them from the first access/sense lines **24**-**27**.

The pattern of lines **56**-**59** is transferred into the programmable material **32** and the third electrode material **34**. Such singulates the programmable material into individual memory cells **60** (only some of which are labeled), and singulates the third electrode material **34** into electrodes **62** (only some of which are labeled).

The memory cells **60** form a memory array; with each memory cell being uniquely addressed through the combination of an access/sense line from the first series under the memory cells (i.e., the access/sense lines **24**-**27**) and an access/sense line from the second series above the memory cells (i.e., the access/sense lines **56**-**59**). In some embodiments, the access/sense lines **24**-**27** may correspond to wordlines, and the access/sense lines **56**-**59** may correspond to bitlines.

The access/sense lines **26** and **57** are diagrammatically illustrated in FIG. **10**D. The lines are shown in dashed-line view to indicate that the lines **26** and **57** are below and above the plane of FIG. **10**D, respectively. The access/sense line **26** has sidewalls **71** extending along the first direction of axis **5**, and the access/sense line **57** has sidewalls **73** extending along the second direction of axis **7**. The memory cells **60** are polygonal structures, and in the shown embodiment are substantially parallelepiped structures (with the term "substantially" meaning that the structures are parallelepiped to within reasonable tolerances of fabrication and measurement). The memory cells have a first pair of opposing sidewalls **75** which are substantially identical to one another and parallel to the sidewalls **73** of access/sense line **57**, and have a second pair of opposing sidewalls **77** which are substantially identical to one another and which extend along a direction which is different than the first and second directions of axes **5** and **7**. In the shown embodiment, the sidewalls **77** are the longest sidewalls of the parallelepiped memory cell structures **60**.

The access/sense lines **26** and **57** are also diagrammatically illustrated in FIG. **10**C. The select devices **44** are illustrated as polygonal structures, and in the shown embodiment are substantially parallelepiped structures having a different shape than the polygonal structures of the memory cells **60**. The select devices **44** have a first pair of opposing sidewalls **81** which are substantially identical to one another and parallel to the sidewalls **71** of access/sense line **26**, and have a second pair of opposing sidewalls **83** which are substantially identical to one another and which extend along a direction which is different than the first and second directions of axes **5** and **7**.

The select devices **44** and memory cells **60** are part of pillars **64** (shown in FIGS. **10**A and **10**B) extending between the access/sense lines **24**-**27** of the first series and the access/sense lines **56**-**59** of the second series. The utilization of multiple different polygonal peripheral shapes for different regions of the pillars may enable the pillars to have enhanced structural integrity as compared to conventional pillars. Such enhanced structural integrity may enable programmable material **32** to be provided to an increased thickness, as discussed above; and/or may provide other benefits, including benefits mentioned above in describing FIGS. **5**-**5**B.

Referring next to FIGS. **11**-**11**D, electrically insulative materials **66** and **68** are formed over and between lines **56**-**59**. The insulative materials **66** and **68** may comprise identical compositions as the materials **28** and **30** described above with reference to FIGS. **3**-**3**B. Accordingly, in some embodiments material **66** may comprise silicon nitride, and material **68** may comprise silicon dioxide. In other embodiments, one or both of materials **66** and **68** may be a different composition than one or both of materials **28** and **30**. In some embodiments materials **66** and **68** may be replaced with a single material, or may be replaced with more than two materials.

FIG. **11**D shows memory cells **60** on a pitch P_2. In some embodiments, such pitch may be less than or equal to about 40 nanometers, less than or equal to about 30 nanometers, etc. In some embodiments, the pitch P_2 may be within a range of from about 10 nanometers to about 40 nanometers; and in some embodiments may be within a range of from about 10 nanometers to about 30 nanometers.

The embodiment of FIGS. **1**-**11** forms memory cells **60** which are configured such that all of the programmable material within the memory cells is configured as one polygonal structure. In other embodiments, the programmable material may be subdivided into two or more regions which are different polygonal shapes relative to one another. An example embodiment process for fabricating the programmable material to comprise two differently-shaped regions is described with reference to FIGS. **12**-**22**.

Referring to FIGS. **12**-**12**B, a portion of a construction **9***a* is illustrated. The construction comprises semiconductor base **4**, electrically insulative material **6**; and a stack **70** formed over the insulative material **6**. Stack **70** includes access/sense material **10**, first electrode material **12**, one or more select device materials **14**, second electrode material **16**, first programmable material **32***a* and third electrode material **34**.

The materials **10**, **12**, **14**, **16** and **34** may be the same as those discussed above with reference to FIGS. **1-5**. The programmable material **32***a* may comprise any of the materials described above with reference to material **32** of FIG. **5**; and in some embodiments may comprise phase change material, such as chalcogenide (for instance, GST). The programmable material **32***a* may be referred to as a first region of programmable material in some embodiments.

Referring to FIGS. **13-13**B, stack **70** is patterned into lines **20-23** extending along the first direction of axis **5**. The patterned access/sense material **10** forms the first series of access/sense lines **24-27**.

Referring to FIGS. **14-14**B, insulative materials **28** and **30** are formed over and between the lines **20-23**.

Referring to FIGS. **15-15**B, the insulative materials **28** and **30** are removed from over lines **20-23**, which exposes a surface of the third electrode material **34** at the tops of the lines. In some embodiments, the materials **28** and **30** may be removed utilizing planarization, such as, for example, chemical-mechanical polishing (CMP).

Referring to FIGS. **16-16**B, second programmable material **32***b* is formed across lines **20-23**; and in the shown embodiment is formed over and directly against the exposed upper surfaces of third electrode material **34**. The programmable material **32***b* may comprise any of the materials described above with reference to material **32** of FIG. **5**; and in some embodiments may comprise phase change material, such as chalcogenide (for instance, GST). The programmable material **32***b* may be referred to as a second region of programmable material to distinguish it from the first region of programmable material corresponding to material **32***a*. In some embodiments, the programmable materials **32***a* and **32***b* may be a same composition as one another, and in other embodiments may be different compositions relative to one another.

A fourth electrode material **72** is formed over programmable material **32***b*. The fourth electrode material may comprise any of the compositions discussed above regarding electrode materials **12**, **16** and **34**; and in some embodiments may be a carbon-containing material.

Referring to FIGS. **17-17**B, the fourth electrode material **72** and programmable material **32***b* are patterned into the diagonal lines **36-42** extending along the diagonal direction of axis **43**.

The diagonal lines **36-42** may be formed with any suitable processing. For instance, a patterned mask (not shown) may be formed over material **72**, a pattern may be transferred from the mask into underlying materials with one or more suitable etches, and then the mask may be removed to leave the construction of FIGS. **17-17**B. The mask may be a lithographic mask (for instance, a photolithographically-patterned photoresist mask) or a sublithographic mask (for instance, a mask formed utilizing pitch-multiplication methodologies).

In the shown embodiment, a pattern of diagonal lines **36-42** is transferred partially into stack **70** (FIGS. **16**A and **16**B), and specifically is transferred through the programmable material **32***a*; the first, second and third electrode materials **12**, **16** and **34**; and the select device materials **14**. Such singulates the select device materials into a plurality of select devices **44** (only some of which are labeled), singulates the first, second and third electrode materials **12**, **16** and **34** into a plurality of first, second and third electrodes **46**, **48** and **74** (only some of which are labeled); and singulates first programmable material **32***a* into first memory cell structures **60***a* (only some of which are labeled). The first memory cell structures are configured as first polygonal structures having a first peripheral shape (specifically, a first parallelepipedal shape in some embodiments), as is discussed in more detail below with reference to FIG. **22**E.

Referring next to FIGS. **18-18**C, electrically insulative materials **50** and **52** are formed over and between lines **36-42** (FIG. **17**).

Referring to FIGS. **19-19**B, the insulative materials **50** and **52** are removed from over lines **36-42**, which exposes a surface of the fourth electrode material **72** at the tops of the lines. In some embodiments, the materials **50** and **52** may be removed utilizing planarization, such as, for example, chemical-mechanical polishing (CMP).

Referring to FIGS. **20-20**C, the second access/sense material **54** is formed across lines **36-42**; and in the shown embodiment is formed over and directly against the exposed upper surfaces of electrode material **72**.

Referring to FIGS. **21-21**C, access/sense material **54** is patterned into the second series of access/sense lines **56-59** extending along the direction of axis **7**. The pattern of lines **56-59** is transferred into the programmable material **32***b* and the fourth electrode material **72**. Such singulates the programmable material **32***b* into individual memory cell structures **60***b* (only some of which are labeled), and singulates the fourth electrode material **72** into electrodes **78** (only some of which are labeled).

The memory cell structures **60***a* and **60***b* are spaced from one another by separating material **34**. The structures **60***a* and **60***b*, together with material **34**, form memory cells **80** of a memory array. The structures **60***a* and **60***b* may be considered to be first and second portions of the programmable material of the memory cells **80**. The material **34** may be kept very thin so that electrical properties of memory cells **80** are primarily dictated by the first and second portions corresponding to structures **60***a* and **60***b*; and in some embodiments the separating material **34** may have a vertical thickness of less than or equal to about 30 nm (such as, for example, a vertical thickness within a range of from about 5 nm to about 30).

In some embodiments, separating material **34** is utilized as an etch stop for the planarization of FIG. **15**. Although separating material **34** is shown remaining in memory cells **80**, in other embodiments material **34** may be entirely removed during or after the planarization of FIG. **15** so that memory cell structures **60***a* and **60***b* directly contact one another; or material **34** may be omitted so that memory cell structures **60***a* and **60***b* directly contact one another.

Each memory cell **80** is uniquely addressed through the combination of an access/sense line from the first series under the memory cells (i.e., the access/sense lines **24-27**) and an access/sense line from the second series above the memory cells (i.e., the access/sense lines **56-59**). In some embodiments, the access/sense lines **24-27** may correspond to wordlines, and the access/sense lines **56-59** may correspond to bitlines.

The access/sense lines **26** and **57** are diagrammatically illustrated in FIG. **21**C. The structures **60***b* are polygonal structures analogous to the structures **60** of FIG. **10**D, and in the shown embodiment are substantially parallelepiped structures having a pair of opposing sidewalls **85** which are substantially identical to one another and which extend along a direction different from the first and second directions of axes **5** and **7**.

Referring next to FIGS. **22-22**E, electrically insulative materials **66** and **68** are formed over and between lines **56-59**.

FIGS. **22**C-E show cross-sections plan views through second memory cell structures **60***b*, first memory cell structures

60*a* and select devices **44**, respectively. Such plan views show that the first and second memory cell structures **60***a* and **60***b* are polygonal structures having different peripheral shapes relative to one another; and show that memory cell structures **60***a* have substantially identical peripheral shapes to select devices **44**.

In some embodiments, structures **60***a* and **60***b* may be referred to as first and second polygonal structures, respectively; and may be considered to have first and second peripheral shapes which are different relative to one another.

The select device structures **44** have sidewalls parallel to sidewalls of the first polygonal structures **60***a*. Specifically, the select devices **44** have sidewalls **91** extending along the same axis **43** as the diagonal lines **36-42** of FIG. **17**, and similarly the memory cell structures **60***a* have sidewalls **93** extending along axis **43**. Such results from structures **44** and **60***a* having been singulated utilizing lines **36-42** as a mask.

The processing of FIGS. **12-22** splits programmable material of memory cells **80** between two portions corresponding to structures **60***a* and **60***b*. Such may advantageously increase structural integrity of pedestals comprising the programmable material, and may enable memory cells to have thicker programmable material than conventional constructions. The thicker programmable material may enable improved electrical separation between different memory states (e.g., "SET" and "RESET" memory states). Also, the thicker programmable material may enable utilization of faster materials, even if such materials have a lower switching field, due to improved separation of memory states achieved utilizing thicker materials.

The inclusion of separating material **34** between the programmable material portions **60***a* and **60***b* within memory cells **80** may be advantageous in tailoring electrical properties of the memory cells for particular applications. In other applications, it may be desired to omit the separating material, and to have the two portions **60***a* and **60***b* directly contacting one another. If the portions **60***a* and **60***b* directly contact one another, such portions may comprise different compositions relative to one another in some embodiments, and may comprise the same compositions as one another in other embodiments. For instance, both of the portions **60***a* and **60***b* may comprise chalcogenide; and in some embodiments the chalcogenide of portion **60***a* may be identical to that of portion **60***b*, while in other embodiments the chalcogenide of one portion may be different from that of the other.

The memory arrays described above with reference to FIGS. **11** and **22** may be considered to be examples of 3-D cross-point memory architecture in some embodiments.

The memory cells and arrays discussed above may be incorporated into electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

Unless specified otherwise, the various materials, substances, compositions, etc. described herein may be formed with any suitable methodologies, either now known or yet to be developed, including, for example, atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), etc.

The terms "dielectric" and "electrically insulative" may be both utilized to describe materials having insulative electrical properties. Both terms are considered synonymous in this disclosure. The utilization of the term "dielectric" in some instances, and the term "electrically insulative" in other instances, is to provide language variation within this disclosure to simplify antecedent basis within the claims that follow, and is not utilized to indicate any significant chemical or electrical differences.

The particular orientation of the various embodiments in the drawings is for illustrative purposes only, and the embodiments may be rotated relative to the shown orientations in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships between various features, regardless of whether the structures are in the particular orientation of the drawings, or are rotated relative to such orientation.

The cross-sectional side views of the accompanying illustrations only show features within the planes of the cross-sections, and do not show materials behind the planes of the cross-sections in order to simplify the drawings. The cross-sectional plan views do show materials below the planes of the plan views.

When a structure is referred to above as being "on" or "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against" another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

Some embodiments include a memory array comprising a first series of access/sense lines extending along a first direction; and a second series of access/sense lines over the first series of access/sense lines and extending along a second direction which is substantially orthogonal to the first direction. The memory array also comprises memory cells vertically between the first and second series of access/sense lines. Each memory cell is uniquely addressed by a combination of an access/sense line from the first series and an access/sense line from the second series. The memory cells comprise programmable material. At least some of the programmable material within each memory cell is a polygonal structure having a sidewall that extends along a third direction which is different from the first and second directions.

Some embodiments include a method of forming a memory array. First access/sense material is formed over a semiconductor substrate. The first access/sense material is patterned into first lines which extend along a first direction. The first lines comprise a first series of access/sense lines. Programmable material is formed over the first lines. The programmable material is patterned into diagonal lines that cross the first lines. The diagonal lines extend along a diagonal direction that is not parallel to the first direction and that is not orthogonal to the first direction. Second access/sense material is formed over the diagonal lines. The second access/sense material is patterned into second lines which extend along a second direction. The second direction is substantially orthogonal to the first direction. The second lines comprise a second series of access/sense lines. A pattern from the second lines is transferred into the programmable material to singulate the programmable material into individual memory cells. The programmable material within the memory cells has sidewalls which extend diagonally relative to sidewalls of the access/sense lines of the first and series. Each of the memory cells is uniquely addressed by a combination of an access/sense line from the first series and an access/sense line from the second series.

Some embodiments include a method of forming a memory array. A stack is formed over a semiconductor substrate. The stack comprises a first region of programmable material over a first access/sense material. The stack is patterned into first lines which extend along a first direction. The first lines comprise a first series of access/sense lines. A second region of programmable material is formed over the first lines. The second region of programmable material is patterned into diagonal lines that cross the first lines. The diagonal lines extend along a diagonal direction that is not parallel to the first direction and that is not orthogonal to the first direction. A pattern from the diagonal lines is transferred into the first region of the programmable material to singulate the first region of the programmable material into first programmable material portions of memory cells. The first programmable material portions are configured as first polygonal structures having a first peripheral shape; Second access/sense material is formed over the diagonal lines. The second access/sense material is patterned into second lines which extend along a second direction. The second direction is substantially orthogonal to the first direction. The second lines comprise a second series of access/sense lines. A pattern from the second lines is transferred into the second region of the programmable material to singulate the second region of the programmable material into second programmable material portions of the memory cells. The second programmable material portions are configured as second polygonal structures having a second peripheral shape different from the first peripheral shape. Each of the memory cells is uniquely addressed by a combination of an access/sense line from the first series and an access/sense line from the second series.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

I claim:

1. A memory array, comprising:

a first series of access/sense lines extending along a first lateral direction relative to an upper surface of a substrate;

a second series of access/sense lines elevationally, over the first series of access/sense lines and extending along a second lateral direction which is substantially orthogonal to the first lateral direction; and

memory cells extending vertically upward relative to the upper surface and being disposed between the first and second series of access/sense lines; each memory cell being uniquely addressed by a combination of an access/sense line from the first series and an access/sense line from the second series; the memory cells comprising programmable material; at least some of the programmable material within each memory cell being a polygonal structure having a sidewall that extends along a third lateral direction which is different from the first and second lateral directions.

2. The memory array of claim **1** wherein the polygonal structure is substantially a parallelepiped.

3. The memory array of claim **2** wherein the sidewall is one of a pair of substantially identical longest sidewalls of the parallelepiped.

4. The memory array of claim **1** wherein the programmable material comprises phase change material.

5. The memory array of claim **1** wherein the programmable material comprises chalcogenide.

6. The memory array of claim **1** wherein all of the programmable material within each memory cell is configured as said polygonal structure.

7. The memory array of claim comprising select devices between the memory cells and the first access/sense lines; the select devices having sidewalls extending along the third lateral direction.

8. The memory array of claim **1** wherein the polygonal structure is a second polygonal structure, wherein only some of the programmable material within each memory cell is configured as said second polygonal structure, and wherein some of the programmable material within each memory cell is configured as a first polygonal structure beneath said second polygonal structure and having a different shape than the second polygonal structure.

9. The memory array of claim **8** wherein a portion of the programmable material configured as the first polygonal structure is a first portion of the programmable material of the memory cell; wherein a portion of the programmable material configured as the second polygonal structure is a second portion of the programmable material of the memory cell; and wherein each memory cell further comprises a separating material between the first and second portions.

10. The memory array of claim **9** further comprising select devices between the memory cells and the first access/sense lines; the select devices having sidewalls parallel to sidewalls of the first polygonal structures.

11. The memory array of claim **9** wherein the first and second portions are a same composition as one another.

12. The memory array of claim **9** wherein the first and second portions are different compositions relative to one another.

13. The memory array of claim **9** wherein the separating material comprises carbon.

14. The memory array of claim **8** wherein a portion of the programmable material configured as the first polygonal structure is a first portion of the programmable material of the memory cell; wherein a portion of the programmable material configured as the second polygonal structure is a second portion of the programmable material of a memory cell; and wherein the second portion is a different composition from the first portion.

15. The memory array of claim **14** wherein the first and second portions comprise chalcogenide.

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